

Low Power Single 2-Input Positive NOR-Gate

Description

This single 2-input positive-NOR gate is designed for 0.8-V to 3.6-V VCC operation.

The FLG74UP1G02 performs the Boolean function $Y = \overline{A \times B}$ in positive logic.

The CMOS device has high output drive while maintaining low static power dissipation over abroad VCC operating range.

The FLG74UP1G02 device is available in a variety of packages, including SOT23-5, SC70.

Features

- Inputs Accept Voltages 0.8V to 3.6 V
- Max Tpd of 5 ns at 3.3 V
- Low Static-Consumption, 0.5- μ A Max I_{CC}
- Low Noise Overshoot and Undershoot < 10% of V_{CC}
- Ioff Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at Input ($V_{hys} = 250\text{mV}$ Typical 3.3V)

- 3.6V I/O Tolerant to Support Mixed-Mode Signal Operation
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 1000-V Charged-Device Model (C101)

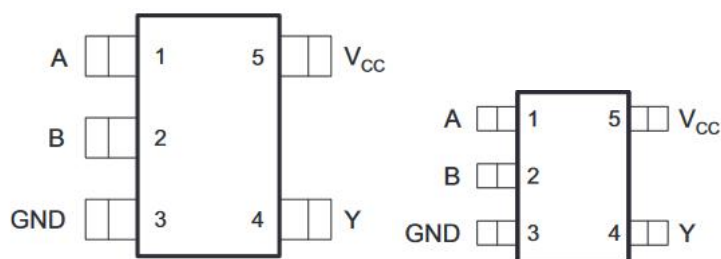
Applications

- ATCA Solutions
- Active Noise Cancellation (ANC)
- Barcode Scanner
- Blood Pressure Monitor
- CPAP Machine
- Cable Solutions
- DLP 3DMachine Vision, Hyperspectral Imaging, Optical Networking, and Spectroscopy
- E-Book
- Embedded PC
- Field Transmitter : Temperature or Pressure Sensor
- Fingerprint Biometrics
- HVAC: Heating, Ventilating, and Air Conditioning

Order information

Mode	Package	Ordering Number	Packing Option
FLG74UP1G02	SOT23-5	FLG74AUP1G02YSOT235G/TR	Tape and Reel,3000
	SC70	FLG74AUP1G02YSC70G/TR	Tape and Reel,3000

Pin Configuration



Simplified Schematic



Pin Assignment

Pin Name	Pin No.	Pin Function
A	1	Input
B	2	Input
GND	3	Ground
Y	4	Output
VCC	5	Power Pin

Absolute Maximum Ratings (Note1)

- V_{CC} ----- -0.5V to +4.6V
- V_I ----- -0.5V to +4.6V
- V_O (Voltage range applied to any output in the high-impedance or power-off state) ----- -0.3V to +4.6V
- V_O (Voltage range applied to any output in the high or slow state) ----- -0.3V to $V_{CC}+0.3V$
- Input clamp current ----- -50mA
- Output clamp current ----- -50mA
- Continuous output current ----- $\pm 20mA$
- Storage Temperature ----- $-65^{\circ}C$ to $150^{\circ}C$

Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply voltage	V_{CC}	Operating	0.8		3.6	V
Input voltage	V_I		0		3.6	V
Output voltage	V_O		0		V_{CC}	V
High- level input voltage	V_{IH}	$V_{CC} = 0.8V$	V_{CC}			V
		$V_{CC} = 1.1V$ to $1.95V$	$0.65 \times V_{CC}$			
		$V_{CC} = 2.3V$ to $2.7V$	1.6			
		$V_{CC} = 3V$ to $3.6V$	2			
Low- level input voltage	V_{IL}	$V_{CC} = 0.8V$			0	V
		$V_{CC} = 1.1V$ to $1.95V$			$0.35 \times V_{CC}$	
		$V_{CC} = 2.3V$ to $2.7V$			0.7	
		$V_{CC} = 3V$ to $3.6V$			0.9	
High- level output current	I_{OH}	$V_{CC} = 0.8V$			-20	uA
		$V_{CC} = 1.1V$			-1.1	mA
		$V_{CC} = 1.4V$			-1.7	
		$V_{CC} = 1.65V$			-1.9	
		$V_{CC} = 2.3V$			-3.1	
		$V_{CC} = 3V$			-4	
Low- level output current	I_{OL}	$V_{CC} = 0.8V$			20	uA
		$V_{CC} = 1.1V$			1.1	mA
		$V_{CC} = 1.4V$			1.7	
		$V_{CC} = 1.65V$			1.9	
		$V_{CC} = 2.3V$			3.1	
		$V_{CC} = 3V$			4	
Input transition rise or fall rate	$\Delta T/\Delta V$	$V_{CC} = 0.8V$ to $3.6V$			200	ns/V
Operating temperature	T_A		-40		85	$^{\circ}C$

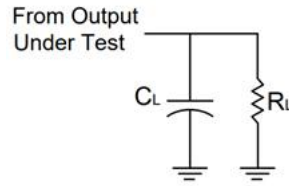
Electrical Characteristics

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
High- level output voltage	V _{OH}	V _{CC} = 0.8~3.6V, I _{OH} = -20uA	V _{CC} -0.1			V
		V _{CC} = 1.1V, I _{OH} = -1.1mA	0.75×V _{CC}			
		V _{CC} = 1.4V, I _{OH} = -1.7mA	1.11			
		V _{CC} = 1.65V, I _{OH} = -1.9mA	1.32			
		V _{CC} = 2.3V, I _{OH} = -2.3mA	2.05			
		V _{CC} = 2.3V, I _{OH} = -3.1mA	1.9			
		V _{CC} = 3V, I _{OH} = -2.7mA	2.72			
		V _{CC} = 3V, I _{OH} = -4mA	2.6			
Low- level output voltage	V _{OL}	V _{CC} = 0.8~3.6V, I _{OL} = 20uA			0.1	V
		V _{CC} = 1.1V, I _{OL} = 1.1mA			0.3×V _{CC}	
		V _{CC} = 1.4V, I _{OL} = 1.7mA			0.31	
		V _{CC} = 1.65V, I _{OL} = 1.9mA			0.31	
		V _{CC} = 2.3V, I _{OL} = 2.3mA			0.31	
		V _{CC} = 2.3V, I _{OL} = 3.1mA			0.44	
		V _{CC} = 3V, I _{OL} = 2.7mA			0.31	
		V _{CC} = 3V, I _{OL} = 4mA			0.44	
Input leakage current	I _I	V _{IN} = 3.6V or GND, V _{CC} = 0~3.6V			0.1	uA
Power off leakage current	I _{OFF}	V _I or V _O =0V to 3.6V, V _{CC} =0V			0.2	uA
Supply current	I _{CC}	V _I = GND or (V _{CC} to 3.6V), I _{OUT} =0, V _{CC} =0.8~3.6V			0.5	uA
Additional supply current per input pin	ΔI _{CC}	V _I = V _{CC} -0.6V, I _{OUT} =0			40	uA

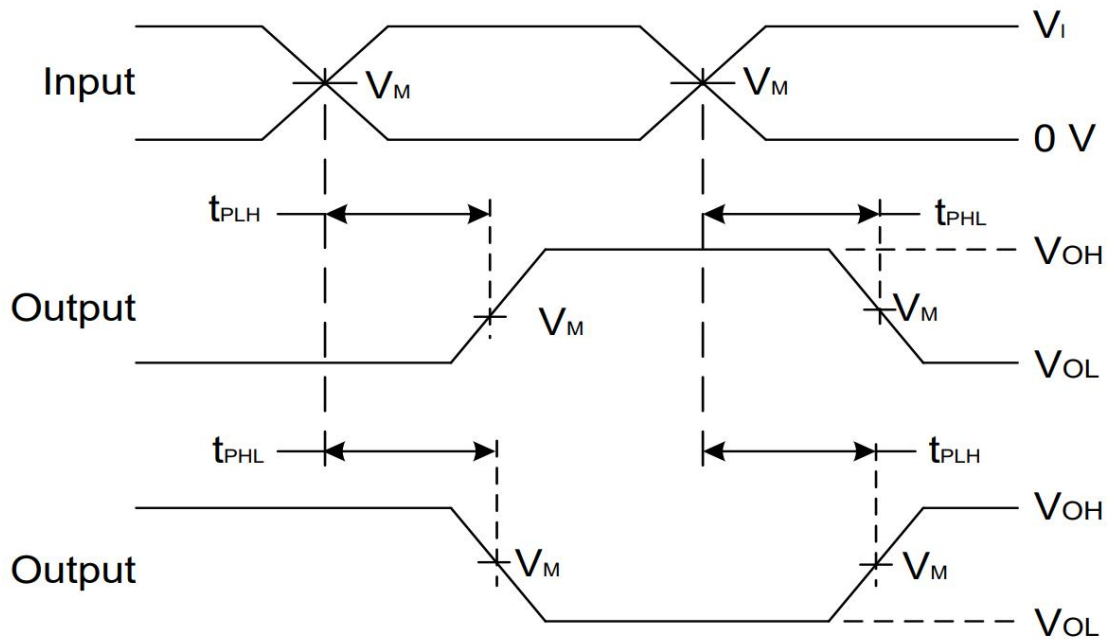
Switching Characteristics

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Propagation delay from input(A or B) to output(Y)	T _{PD}	V _{CC} = 0.8V		25		ns
		V _{CC} = 1.2V±0.1V	3.6	9.9	16.5	
		V _{CC} = 1.5V±0.1V	2.3	7.2	11.3	
		V _{CC} = 1.8V±0.15V	1.6	5.8	8.9	
		V _{CC} = 2.5V±0.2V	1	4.3	6.1	
		V _{CC} = 3.3V±0.3V	1	3.4	5	

Parameter Measurement Information



V _{CC}	INPUTS		V _M	C _L	R _L
	V _I	t _r /t _f			
0.8V	V _{CC}	≅ 2ns	V _{CC} /2	15pF	1MΩ
1.2V ± 0.1V	V _{CC}	≅ 2ns	V _{CC} /2	15pF	1MΩ
1.5V ± 0.1V	V _{CC}	≅ 2ns	V _{CC} /2	15pF	1MΩ
1.8V ± 0.15V	V _{CC}	≅ 2ns	V _{CC} /2	15pF	1MΩ
2.5V ± 0.2V	3V	≅ 2.5ns	1.5V	15pF	1MΩ
3.3V ± 0.3V	V _{CC}	≅ 2.5ns	V _{CC} /2	15pF	1MΩ



Voltage Waveform Propagation Delay Times
Inverting and Non Inverting Outputs

- Notes: A. C_L includes probe and jig capacitance
 B. All pulses and supplied at pulse repetition rate ≅ 10MHz
 C. The Inputs are measured separately one transition per measurement
 D. t_{PLH} and t_{PHL} are the same as t_{PD}

IC Operation Information

Basic Operation

The FLG74UP1G02 device contains one 2-input positive NAND gate device and performs the Boolean function $Y = \overline{A \times B}$ or $Y = \overline{A} + \overline{B}$. The AUP family of devices has quiescent power consumption less than 1 μ A. This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered. The Ioff feature also allows for live insertion.

Function Block Diagram



Feature Description

- Wide operating V_{CC} range of 0.8V to 3.6V.
- 3.6-V I/O tolerant to support down translation.
- Input hysteresis allows slow input transition and better switching noise immunity at the input.
- Ioff feature allows voltages on the inputs and outputs when V_{CC} is 0 V.
- Low noise due to slower edge rates.

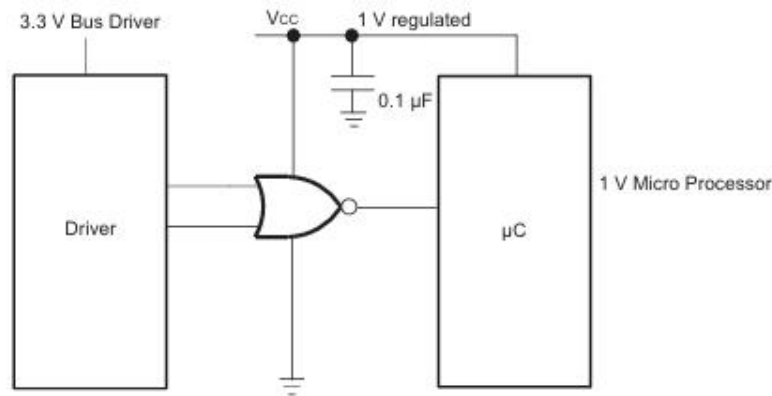
Device Functional Table

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

IC Application Information

The AUP family is the solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity. It has a small amount of hysteresis built in allowing for slower or noisy input signals. The lowered drive produces slower edges and prevents overshoot and undershoot on the outputs.

Typical Application



Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits

Detailed Design Procedure

1. Recommended Input conditions:

- Rise time and fall time specs. See ($\Delta t/\Delta V$)
- Specified high and low levels. See (V_{IH} and V_{IL})
- Inputs are overvoltage tolerant allowing them to go as high as 3.6 V at any valid VCC

2. Recommended output conditions:

- Load currents should not exceed 20 mA on the output and 50 mA total for the part
- Outputs should not be pulled above VCC

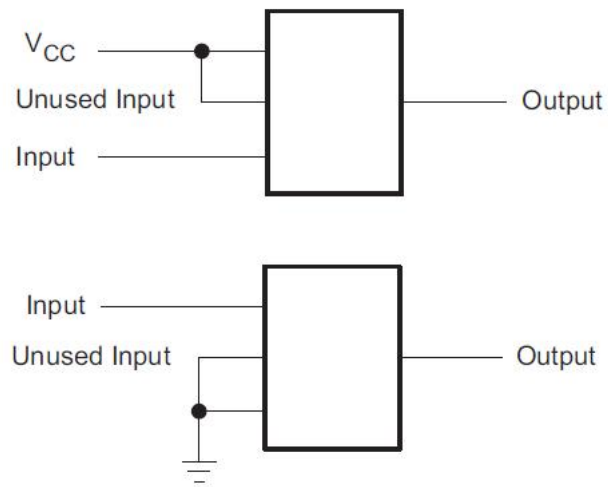
Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the Recommended Operating Conditions table. Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended; if there are multiple VCC pins, then 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and a 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

Layout Considerations

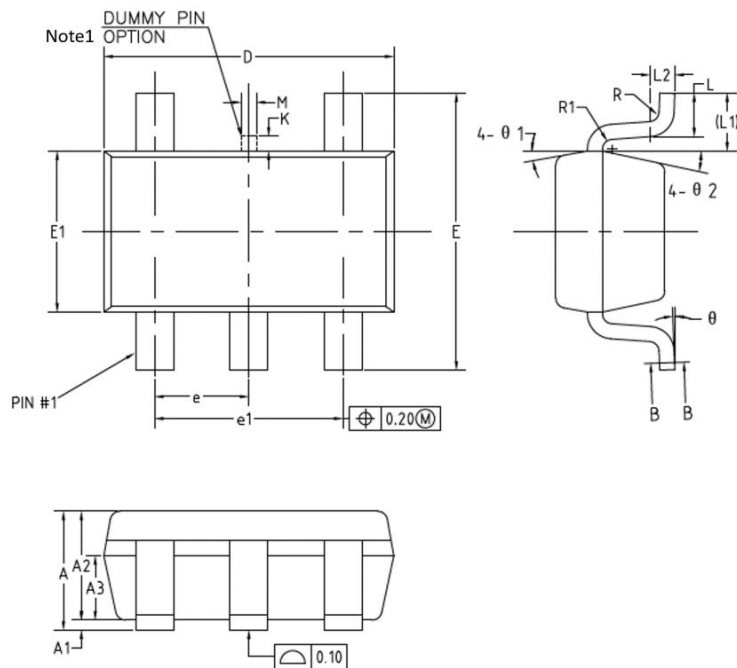
In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Below figure specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or VCC, whichever makes more sense or is

more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.



Package Information

(1) Package Type: SOT23-5

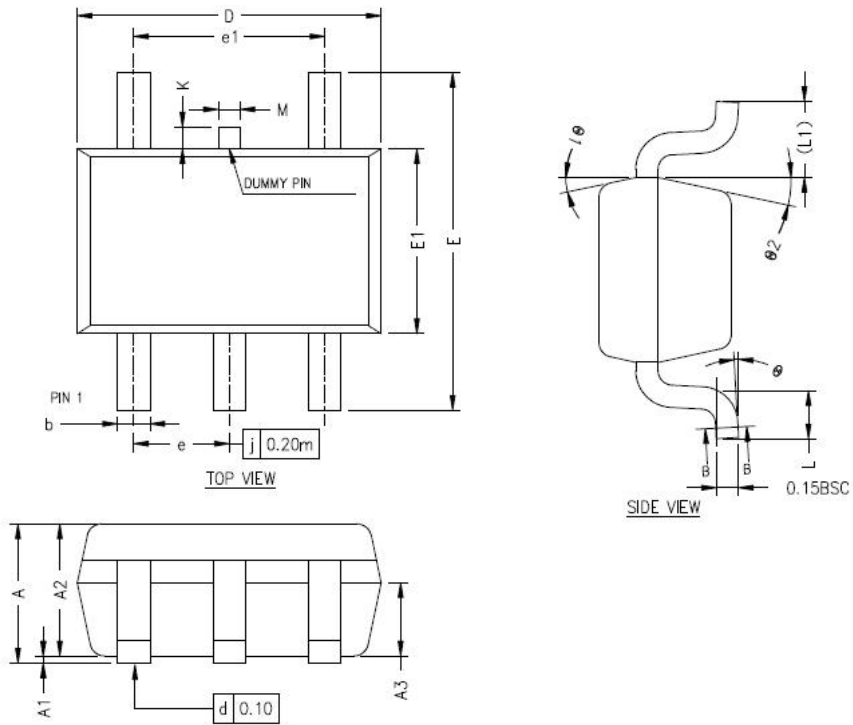


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.25
A1	0	—	0.15
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
⚠ b	0.34	—	0.45
⚠ b1	0.34	0.38	0.41
⚠ c	0.12	—	0.20
⚠ c1	0.12	0.15	0.16
D	2.826	2.926	3.026
E	2.60	2.80	3.00
⚠ E1	1.526	1.626	1.700
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
⚠ K	0	—	0.20
L	0.30	0.40	0.60
L1	0.59REF		
L2	0.25BSC		
⚠ M	0.10	0.15	0.20
R	0.05	—	0.20
R1	0.05	—	0.20
θ	0°	—	8°
θ 1	8°	10°	12°
θ 2	10°	12°	14°

Notes: 1. Dummy pin may differ or may not be present.

(2) Package Type: SC70



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.80	—	1.10
A1	0	—	0.10
A2	0.80	0.90	1.00
A3	0.40	0.50	0.60
b	0.17	—	0.30
b1	0.17	0.22	0.25
\triangle_3 c	0.12	—	0.20
\triangle_3 c1	0.12	0.15	0.16
D	2.02	2.07	2.12
E	2.20	2.30	2.40
E1	1.21	1.26	1.31
e	0.60	0.65	0.70
e1	1.20	1.30	1.40
L	0.26	0.33	0.46
L1	0.52REF		
\triangle_2 M	0.10	0.15	0.20
\triangle_2 K	0	—	0.20
θ	0°	—	8°
θ_1	10°	12°	14°
θ_2	10°	12°	14°

Important Notice And Disclaimer

- We reserves the right to change the instruction manual without prior notice.
- Any semiconductor product has a certain possibility of failure or malfunction under specific conditions. The buyer is responsible for complying with safety standards and taking safety measures when using our products for system design and overall manufacturing to avoid potential failure risks that may cause personal injury or property damage.
- The improvement of product quality is endless, our company will be dedicated to provide customers with better products.