Low-Power Single Bus Buffer Gate With 3-State Output

Description

The bus buffer gate is designed for 0.8-V to 3.6-V VCC operation.

The FLG74AUP1G125 device is a single line driver with a 3-state output. The output is disabled when the output-enable ($\overline{OE}$) input is high.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ must be tied to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The FLG74AUP1G125 device is available in a

variety of packages, including SOT23-5, SC70.

Features

- Inputs Accept Voltages 0.8V to 3.6 V
- Max Tpd of 4.7 ns at 3.3 V
- Low Static-Consumption, 0.5-μA Max I_{CC}
- Low Noise Overshoot and Undershoot < 10% of V_{CC}
- Ioff Supports Live Insertion,Partial-Power-Down Mode, and Back-Drive Protection
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at Input(V_{hys}= 250mV Typical 3.3V)
- 3.6V I/O Tolerant to Support Mixed-Mode Signal Operation
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

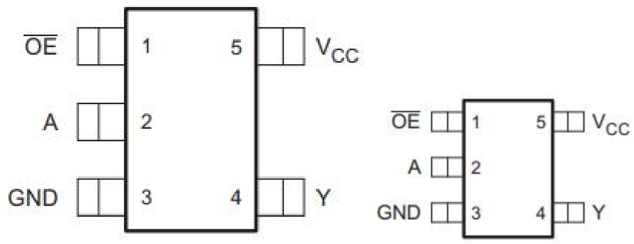
Applications

- Audio Dock: Portable
- BluRay™ Players and Home Theaters
- Personal Digital Assistant (PDA)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Power: Telecom/Server AC/DC Supply: Single
- TV: LCD/Digital and High-Definition (HDTV)
- Tablet: Enterprise
- Wireless Headsets, Keyboards and Mice

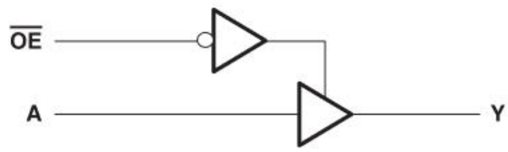
Order information

Mode	Package	Ordering Number	Packing Option
FLG74AUP1G125	SOT23-5	FLG74AUP1G125YSOT235G/TR	Tape and Reel,3000
	SC70	FLG74AUP1G125YSC70G/TR	Tape and Reel,3000

Pin Configuration



Simplified Schematic



Pin Assignment

Pin Name	Pin No.	Pin Function
$\overline{OE}$	1	Input
A	2	Input
GND	3	Ground
Y	4	Output
VCC	5	Power Pin

Absolute Maximum Ratings (Note1)

- V_{CC} -- -0. 5V to + 4.6V
- V_I --- - 0. 5V t o + 4. 6V
- V_O (Voltage range applied to any output in the high-impedance or power-off state) ---------------- - 0. 3V to + 4. 6V
- V_O(Voltage range applied to any output in the high or slow state)---------------------------------- -0.3V to V_{CC}+0.3V
- Input clamp current -- -50mA
- Output clamp current --- -50mA
- Continuous output current --- ±20mA
- Storage Temperature -- -65℃ to 150℃

Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply voltage	V_{CC}	Operating	0.8		3.6	V
Input voltage	V_I		0		3.6	V
Output voltage	V_O		0		VCC	V
High- level input voltage	V_{IH}	V_{CC} = 0.8V	V_{CC}			V
		V_{CC} = 1.1V to 1.95V	0.65×V_{CC}			
		V_{CC} = 2.3V to 2.7V	1.6			
		V_{CC} = 3V to 3.6V	2			
Low- level input voltage	V_{IL}	V_{CC} = 0.8V			0	V
		V_{CC} = 1.1V to 1.95V			0.35×V_{CC}	
		V_{CC} = 2.3V to 2.7V			0.7	
		V_{CC} = 3V to 3.6V			0.9	
High- level output current	I_{OH}	V_{CC} = 0.8V			-20	uA
		V_{CC} = 1.1V			-1.1	mA
		V_{CC} = 1.4V			-1.7	
		V_{CC} = 1.65V			-1.9	
		V_{CC} = 2.3V			-3.1	
		V_{CC} = 3V			-4	
Low- level output current	I_{OL}	V_{CC} = 0.8V			20	uA
		V_{CC} = 1.1V			1.1	mA
		V_{CC} = 1.4V			1.7	
		V_{CC} = 1.65V			1.9	
		V_{CC} = 2.3V			3.1	
		V_{CC} = 3V			4	
Input transition rise or fall rate	△T/△V	V_{CC} = 0.8V to 3.6V			200	ns/V
Operating temperature	T_A		-40		85	℃

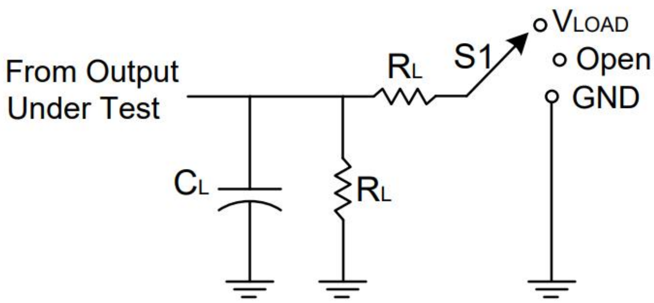
Electrical Characteristics

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
High- level output voltage	V_{OH}	V_{CC} = 0.8~3.6V, I_{OH}= -20uA	V_{CC}-0.1			V
		V_{CC} = 1.1V, I_{OH}= -1.1mA	0.75×V_{CC}			
		V_{CC} = 1.4V, I_{OH}= -1.7mA	1.11			
		V_{CC} = 1.65V, I_{OH}= -1.9mA	1.32			
		V_{CC} = 2.3V, I_{OH}= -2.3mA	2.05			
		V_{CC} = 2.3V, I_{OH}= -3.1mA	1.9			
		V_{CC} = 3V, I_{OH}= -2.7mA	2.72			
		V_{CC} = 3V, I_{OH}= -4mA	2.6			
Low- level output voltage	V_{OL}	V_{CC} = 0.8~3.6V, I_{OL}= 20uA			0.1	V
		V_{CC} = 1.1V, I_{OL}= 1.1mA			0.3×V_{CC}	
		V_{CC} = 1.4V, I_{OL}= 1.7mA			0.31	
		V_{CC} = 1.65V, I_{OL}= 1.9mA			0.31	
		V_{CC} = 2.3V, I_{OL}= 2.3mA			0.31	
		V_{CC} = 2.3V, I_{OL}= 3.1mA			0.44	
		V_{CC} = 3V, I_{OL}= 2.7mA			0.31	
		V_{CC} = 3V, I_{OL}= 4mA			0.44	
Input leakage current	I_I	V_{IN}= 3.6V or GND, V_{CC}= 0~3.6V			0.1	uA
Power off leakage current	I_{OFF}	V_I or V_O=0V to 3.6V, V_{CC}=0V			0.2	uA
Supply current	I_{CC}	V_I= GND or (V_{CC} to 3.6V), I_{OUT}=0,V_{CC}=0.8~3.6V			0.5	uA
Additional supply current per input pin	△I_{CC}	V_I= V_{CC}-0.6V, I_{OUT}=0			40	uA

Switching Characteristics

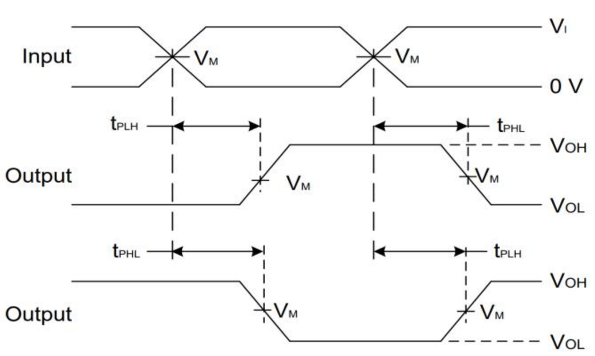
Parameter	From Input	To Output	Test Conditions	Min.	Typ.	Max.	Unit
T_{PD}	A	Y	V_{CC} = 0.8V		22.5		ns
			V_{CC} = 1.2V±0.1V	5.8	9.3	15.1	
			V_{CC} = 1.5V±0.1V	4.4	6.6	10.2	
			V_{CC} = 1.8V±0.15V	3.5	5.3	8.3	
			V_{CC} = 2.5V±0.2V	2.7	3.9	5.8	
			V_{CC} = 3.3V±0.3V	2.4	3.2	4.7	
T_{en}	$\overline{OE}$	Y	V_{CC} = 0.8V		25.2		ns
			V_{CC} = 1.2V±0.1V	7	11.3	18.1	
			V_{CC} = 1.5V±0.1V	5.5	8.1	12.2	
			V_{CC} = 1.8V±0.15V	4.3	6.5	10.1	
			V_{CC} = 2.5V±0.2V	3.4	4.8	7.1	
			V_{CC} = 3.3V±0.3V	2.9	4.1	5.9	
T_{dis}	$\overline{OE}$	Y	V_{CC} = 0.8V		14		ns
			V_{CC} = 1.2V±0.1V	3.7	5.8	8.2	
			V_{CC} = 1.5V±0.1V	5.5	3.9	5.9	
			V_{CC} = 1.8V±0.15V	3.3	4.5	6.6	
			V_{CC} = 2.5V±0.2V	2.3	3.2	4.3	
			V_{CC} = 3.3V±0.3V	2.4	4.8	6.2	

Parameter Measurement Information

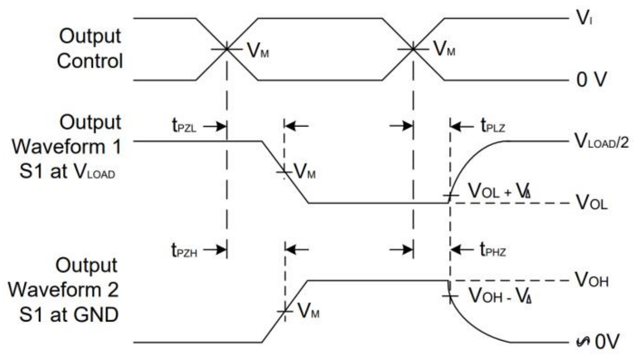


TEST	S1	R_L
t_{PLH}/t_{PHL}	Open	1MΩ
t_{PLZ}/t_{PZL}	V_{LOAD}	5KΩ
t_{PHZ}/t_{PZH}	GND	5KΩ

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	V△
	V_I	t_r/t_f				
0.8V	V_{CC}	≦3ns	$V_{CC}/2$	2 × V_{CC}	15pF	0.1V
1.2V ± 0.1V	V_{CC}	≦3ns	$V_{CC}/2$	2 × V_{CC}	15pF	0.1V
1.5V ± 0.1V	V_{CC}	≦3ns	$V_{CC}/2$	2 × V_{CC}	15pF	0.1V
1.8V ± 0.15V	V_{CC}	≦3ns	$V_{CC}/2$	2 × V_{CC}	15pF	0.15V
2.5V ± 0.2V	V_{CC}	≦3ns	$V_{CC}/2$	2 × V_{CC}	15pF	0.15V
3.3V ± 0.3V	V_{CC}	≦3ns	$V_{CC}/2$	2 × V_{CC}	15pF	0.3V



Voltage Waveform Propagation Delay Times
Inverting and Non Inverting Outputs



Voltage Waveform Enable and DisableTimes
Low- and High-Level Enabling

Notes: A. C_L includes probe and jig capacitance

B. All pulses and supplied at pulse repetition rate≦10MHz

C. The Inputs are measured separately one transition per measurement

D. t_{PLZ} and t_{PHZ} are the same as t_{dis}

E. t_{PZL} and t_{PZH} are the same as t_{en}

F. t_{PLH} and t_{PHL} are the same as t_{PD}

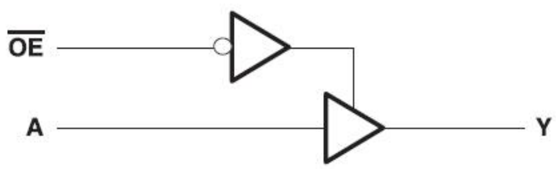
IC Operation Information

Basic Operation

The AUP family is the solution to the industry's low-power needs in battery-powered portable applications. This family of devices is specified for low static and dynamic power consumption across the entire VCC range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity.
This device contains one buffer gate device with output enable control and performs the Boolean function Y = A. This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device, which prevents damage to the device.

To assure the high-impedance state during power up or power down, $\overline{OE}$ must be tied to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Function Block Diagram



Feature Description

- Wide operating V_{CC} range of 0.8V to 3.6V.
- 3.6-V I/O tolerant to support down translation.
- Input hysteresis allows slow input transition and better switching noise immunity at the input.
- Ioff feature allows voltages on the inputs and outputs when V_{CC} is 0 V.
- Low noise due to slower edge rates.

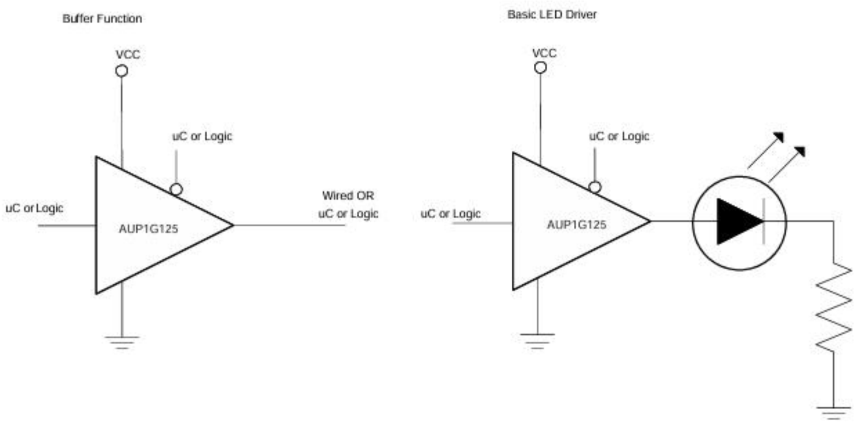
Device Functional Table

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Hi-Z

IC Application Information

The FLG74AUP1G125 is a high drive CMOS device that can be used to implement a high output drive buffer, such as an LED application. It can produce 24 mA of drive current at 3.3 V , which is ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 3.6 V tolerant allowing it to translate down to VCC.

Typical Application



Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads so routing and load conditions should be considered to prevent ringing.

Detailed Design Procedure

1.Recommended Input conditions:

– Rise time and fall time specs. See (Δt/ΔV) in the Recommended Operating Conditions table.

– Specified high and low levels. See (V_{IH} and V_{IL}) in the Recommended Operating Conditions table.

– Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the Recommended Operating Conditions table at any valid V_{CC}

2. Recommended output conditions:

– Load currents should not exceed (I_O max) per output and should not exceed total current (continuous current through V_{CC} or GND) for the part. These limits are located in the Absolute Maximum Ratings table.

– Outputs should not be pulled above V_{CC}

Power Supply Recommendations

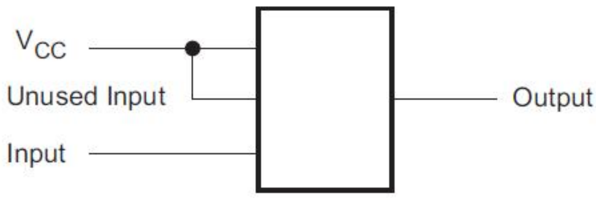
The power supply can be any voltage between the min and max supply voltage rating located in the Recommended Operating Conditions table.

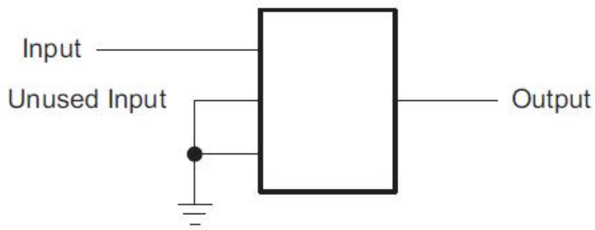
The VCC pin must have a good bypass capacitor to prevent power disturbance. It's recommended to use a 0.1-µF capacitor for this device. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. Install the bypass capacitor as close to the power pin as possible for best results.

Layout Considerations

When using multiple-bit logic devices, inputs should never float.

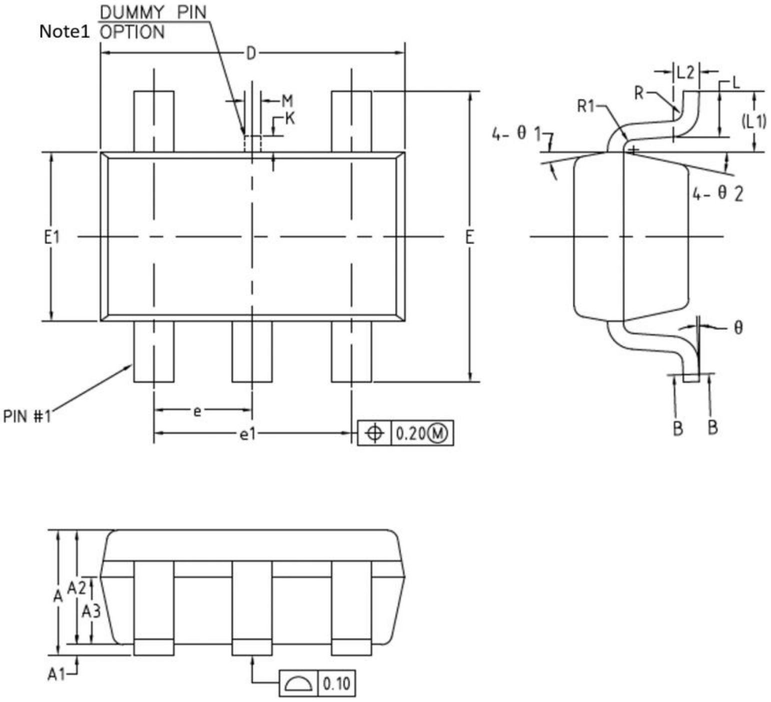
In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Below figure specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or VCC, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.





Package Information

(1) Package Type: SOT23-5

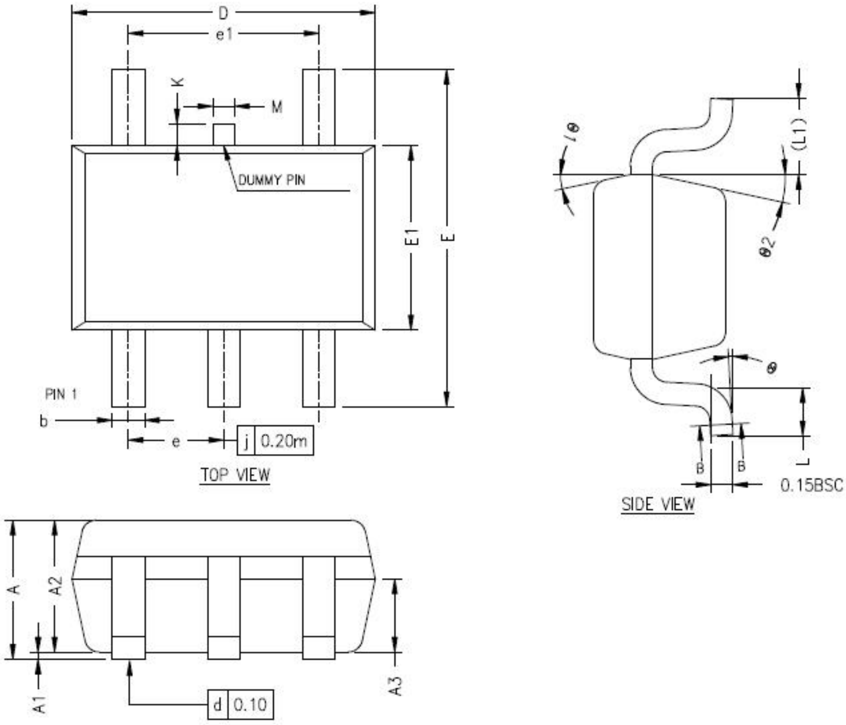


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

	SYMBOL	MIN	NOM	MAX
	A	–	–	1.25
	A1	0	–	0.15
	A2	1.00	1.10	1.20
	A3	0.60	0.65	0.70
△4	b	0.34	–	0.45
△4	b1	0.34	0.38	0.41
△4	c	0.12	–	0.20
△4	c1	0.12	0.15	0.16
	D	2.826	2.926	3.026
	E	2.60	2.80	3.00
△3	E1	1.526	1.626	1.700
	e	0.90	0.95	1.00
	e1	1.80	1.90	2.00
△2	K	0	–	0.20
	L	0.30	0.40	0.60
	L1		0.59REF	
	L2		0.25BSC	
△2	M	0.10	0.15	0.20
	R	0.05	–	0.20
	R1	0.05	–	0.20
	θ	0°	–	8°
	θ 1	8°	10°	12°
	θ 2	10°	12°	14°

Notes: 1. Dummy pin may differ or may not be present.

(2) Package Type: SC70



COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

	SYMBOL	MIN	NOM	MAX
	A	0.80	–	1.10
	A1	0	–	0.10
	A2	0.80	0.90	1.00
	A3	0.40	0.50	0.60
	b	0.17	–	0.30
	b1	0.17	0.22	0.25
△3	c	0.12	–	0.20
△3	c1	0.12	0.15	0.16
	D	2.02	2.07	2.12
	E	2.20	2.30	2.40
	E1	1.21	1.26	1.31
	e	0.60	0.65	0.70
	e1	1.20	1.30	1.40
	L	0.26	0.33	0.46
	L1		0.52REF	
△2	M	0.10	0.15	0.20
△2	K	0	–	0.20
	θ	0°	–	8°
	θ1	10°	12°	14°
	θ2	10°	12°	14°

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