Low Power Dual Inverter with Open-Drain Outputs

Description

This dual inverter buffer and driver is designed for 0.8-V to 3.6-V V_{CC} operation. The CMOS device provides high output drive while maintaining low static power consumption.

The output of the FLG74AUP2G06 device is open-drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

The FLG74AUP2G06 device is available in a variety of packages, including SOT-23-6, SC70-6.

Features

- Inputs Accept Voltages 0.8V to 3.6 V
- Max Tpd of 6 ns at 3.3 V
- Low Static-Consumption, 0.5- μA Max I_{CC}
- Low Noise Overshoot and Undershoot < 10% of V_{CC}
- Ioff Supports Live Insertion,Partial-Power-Down Mode, and Back-Drive Protection
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at Input(V_{hys}= 250mV Typical 3.3V)
- 3.6V I/O Tolerant to Support Mixed-Mode Signal Operation
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

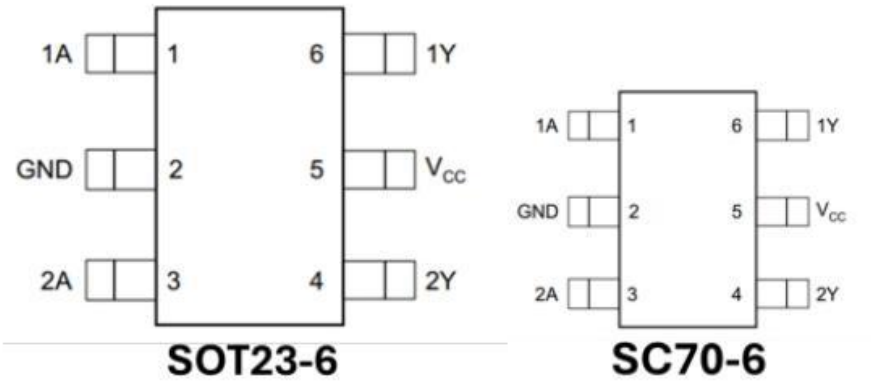
Applications

- AV Receivers
- Smart phone
- Blu-ray Player and Home Theater
- Desktop or Notebook PCs
- Embedded PC
- GPS: Personal Navigation Devices
- Mobile Internet Devices
- Network Projector Front ends
- Portable Media Players
- Smoke Detectors
- Solid State Drive (SSD): Enterprise
- High-Definition (HDTV)
- Tablet: Enterprise
- Audio Dock: Portable

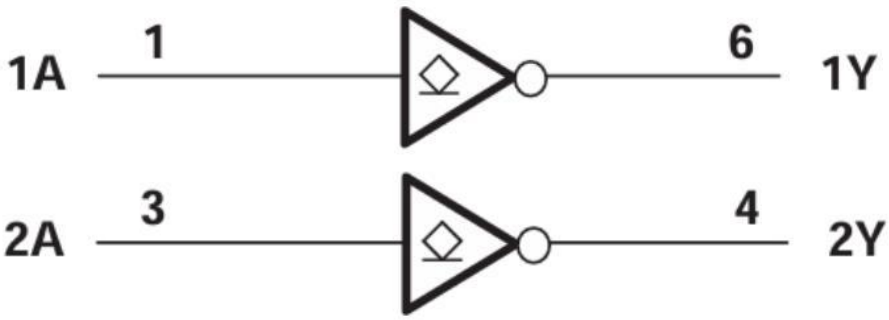
Order information

Mode	Package	Ordering Number	Packing Option
FLG74AUP2G06	SOT-23-6	FLG74AUP2G06YSOT236G/TR	Tape and Reel,3000
	SC70-6	FLG74AUP2G06YSC706G/TR	Tape and Reel,3000

Pin Configuration



Simplified Schematic



Pin Assignment

Pin Name	Pin No.	Pin Function
GND	2	Ground
1A	1	Input 1
2A	3	Input 2
1Y	6	Open-drain output 1
2Y	4	Open-drain output 2
VCC	5	Power pin

Absolute Maximum Ratings (Note1)

- V_{CC} ---------- -0. 5V to + 4.6V
- V_I ---------- - 0. 5V t o + 4. 6V
- V_O (Voltage range applied to any output in the high-impedance or power-off state) ---------- - 0. 3V to + 4. 6V
- V_O(Voltage range applied to any output in the high or slow state)---------- -0.3V to V_{CC}+0.3V
- Input clamp current ---------- -50mA
- Output clamp current ---------- -50mA
- Continuous clamp current ---------- ±20mA
- Storage Temperature ---------- -65℃ to 150℃

Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply voltage	V_{CC}	Operating	0.8		3.6	V
Input voltage	V_I		0		3.6	V
Output voltage	V_O		0		3.6	V
High- level input voltage	V_{IH}	V_{CC} = 0.8V	V_{CC}			V
		V_{CC} = 1.1V to 1.95V	0.65×V_{CC}			
		V_{CC} = 2.3V to 2.7V	1.6			
		V_{CC} = 3V to 3.6V	2			
Low- level input voltage	V_{IL}	V_{CC} = 0.8V			0	V
		V_{CC} = 1.1V to 1.95V			0.35×V_{CC}	
		V_{CC} = 2.3V to 2.7V			0.7	
		V_{CC} = 3V to 3.6V			0.9	
Low- level output current	I_{OL}	V_{CC} = 0.8V			20	uA
		V_{CC} = 1.1V			1.1	mA
		V_{CC} = 1.4V			1.7	
		V_{CC} = 1.65V			1.9	
		V_{CC} = 2.3V			3.1	
		V_{CC} = 3V			4	

Input transition rise or fall rate	△T/△V	V_{CC} = 0.8V to 3.6V			200	ns/V
Operating temperature	T_A		-40		85	℃

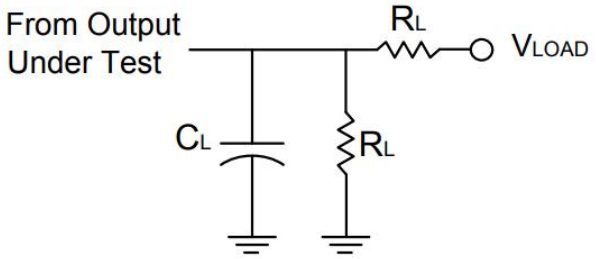
Electrical Characteristics

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Low- level output voltage	V_{OL}	V_{CC} = 0.8~3.6V, I_{OL}= 20uA			0.1	V
		V_{CC} = 1.1V, I_{OL}= 1.1mA			0.3×V_{CC}	
		V_{CC} = 1.4V, I_{OL}= 1.7mA			0.31	
		V_{CC} = 1.65V, I_{OL}= 1.9mA			0.31	
		V_{CC} = 2.3V, I_{OL}= 2.3mA			0.31	
		V_{CC} = 2.3V, I_{OL}= 3.1mA			0.44	
		V_{CC} = 3V, I_{OL}= 2.7mA			0.31	
		V_{CC} = 3V, I_{OL}= 4mA			0.44	
Input leakage current	I_I	V_{IN}= 3.6V or GND, V_{CC}= 0~3.6V			0.1	uA
Power off leakage current	I_{OFF}	V_I or V_O=0V to 3.6V, V_{CC}=0V			0.2	uA
Supply current	I_{CC}	V_I= GND or (V_{CC} to 3.6V), I_{OUT}=0,V_{CC}=0.8~3.6V			0.5	uA
Additional supply current per input pin	△I_{CC}	V_I= V_{CC}-0.6V, I_{OUT}=0			40	uA

Switching Characteristics

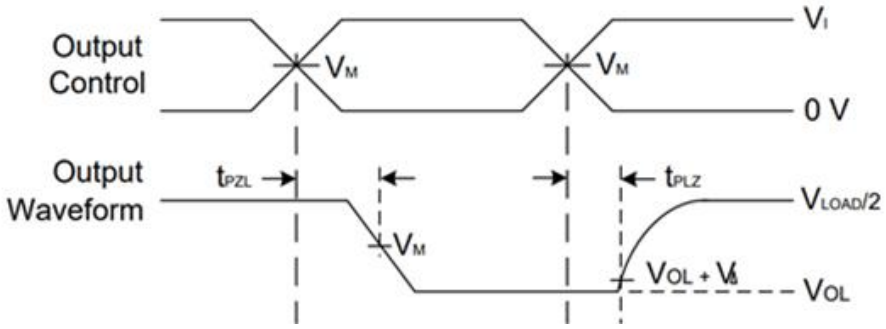
Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Propagation delay from input(A or B) to output(Y)	T_{PD}	V_{CC} = 0.8V	C_L=15pF		17.4		ns
		V_{CC} = 1.2V±0.1V		4.9	12	12..2	
		V_{CC} = 1.5V±0.1V		3.5	5	7.7	
		V_{CC} = 1.8V±0.15V		3.2	4.8	6.6	
		V_{CC} = 2.5V±0.2V		2.5	3.5	4.5	
		V_{CC} = 3.3V±0.3V		2	3.8	6	

Parameter Measurement Information



TEST	Condition
t_{PLZ}	V_{LOAD}
t_{PZL}	V_{LOAD}

V_{CC}	INPUTS		V_M	C_L	R_L
	V_I	t_r/t_f			
0.8V	V_{CC}	≦2ns	$V_{CC}/2$	15pF	5KΩ
1.2V ± 0.1V	V_{CC}	≦2ns	$V_{CC}/2$	15pF	5KΩ
1.5V ± 0.1V	V_{CC}	≦2ns	$V_{CC}/2$	15pF	5KΩ
1.8V ± 0.15V	V_{CC}	≦2ns	$V_{CC}/2$	15pF	5KΩ
2.5V ± 0.2V	3V	≦2.5ns	1.5V	15pF	5KΩ
3.3V ± 0.3V	V_{CC}	≦2.5ns	$V_{CC}/2$	15pF	5KΩ



Voltage Waveform Enable and DisableTimes

Low- and High-Level Enabling

Notes:A. C_L includes probe and jig capacitance

B. All pulses and supplied at pulse repetition rate≦ 10MHz

C. The Inputs are measured one at a time with one transition per measurement

D. For the open drain device t_{PLZ} and t_{PZL} are the same as t_{PD}

E. t_{PZL} is measured at V_M

F. t_{PLZ} is measured at V_{OL} + V△

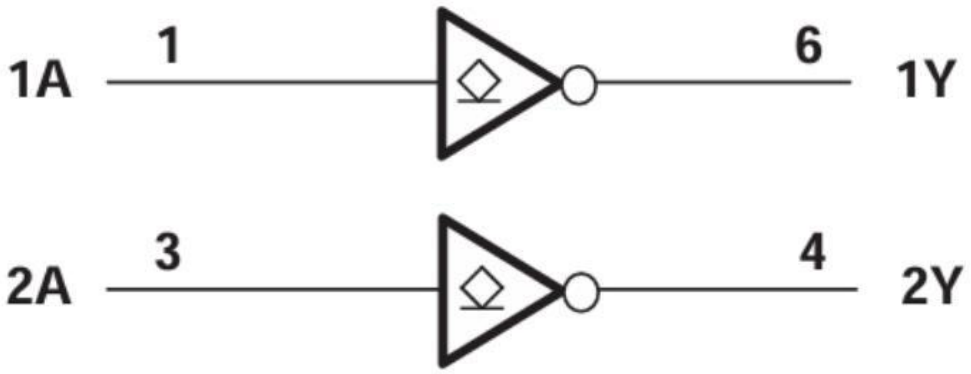
IC Operation Information

Basic Operation

The output of this single inverter buffer/driver is open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered. The Ioff feature also allows for live insertion.

Function Block Diagram



Feature Description

- Wide operating V_{CC} range of 0.8V to 3.6V.
- 3.6-V I/O tolerant to support down translation.
- Input hysteresis allows slow input transition and better switching noise immunity at the input.
- Ioff feature allows voltages on the inputs and outputs when V_{CC} is 0 V.
- Low noise due to slower edge rates.

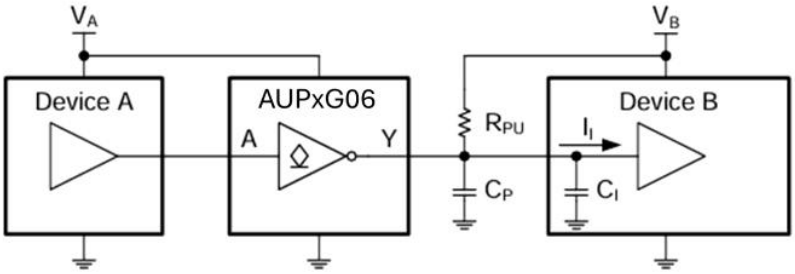
Device Functional Table

INPUTS A	OUTPUT Y
L	Hi-Z
H	L

IC Application Information

Open-drain devices are very commonly used for voltage level translation. In this application, the FLG74AUP2G06 is used to translate a 1.8-V output from device A to a 3.3-V input on device B

Typical Application



Design Requirements

This device has standard CMOS input, so be careful to avoid slow or floating inputs that might cause oscillation or excessive current.

This device has an open-drain output, which means that the output enters a high-impedance state when a normal CMOS device would drive the output high. A pull-up resistor must be added to the output for an open drain device to have a high output. The selection of this pull-up resistor is detailed in the next section

Detailed Design Procedure

1.Recommended Input conditions:

– For specified high and low levels, see VIH and VIL in the Electrical Characteristics table

– Inputs are overvoltage tolerant allowing them to go as high as $V_{I(max)}$ in the Absolute Maximum Ratings table at any valid VCC.

2. Recommended output conditions:

– Output voltage must not exceed $V_{O(max)}$ as specified in the Absolute Maximum Ratings table

– Pull-up resistor (R) selection depends on three primary factors: desired output high voltage (V_{OH}), which is directly related to total leakage current into the FLG74AUP2G06 and the peripheral device's input (I_L), desired 0 to 90% rising edge time (tr), which is directly related to the parasitic line capacitance (C_P), and the maximum current during low output (I_{OL}), which is directly related to the supply value. These three equations govern pull-up resistor selection

– $R \leq (V_{CC} - V_{OH}) / I_L$

– $R \leq tr / (2.3 \times C_P)$

– $R \geq V_{CC} / I_{OL(max)}$

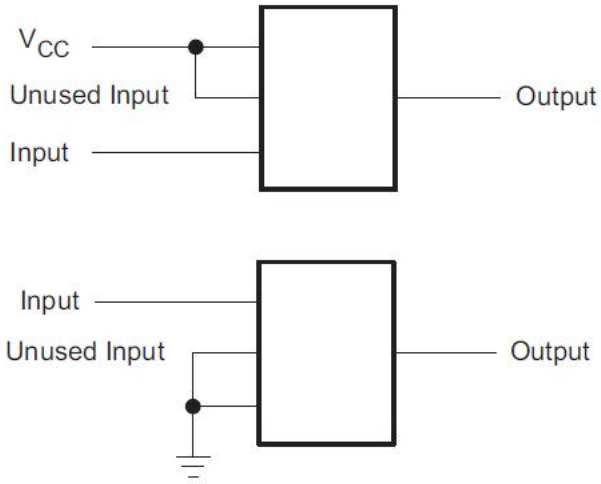
Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the Recommended Operating Conditions table. Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended; if there are multiple VCC pins, then 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and a 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

Layout Considerations

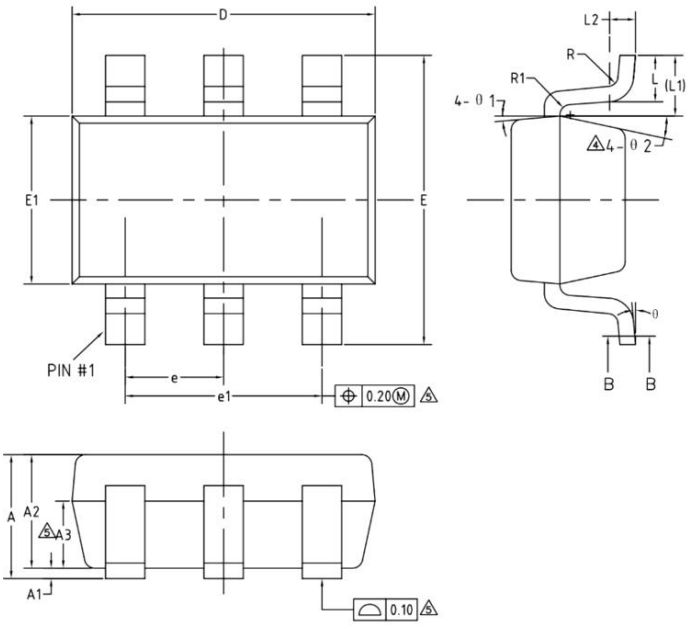
When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Below figure specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or VCC, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.



Package Information

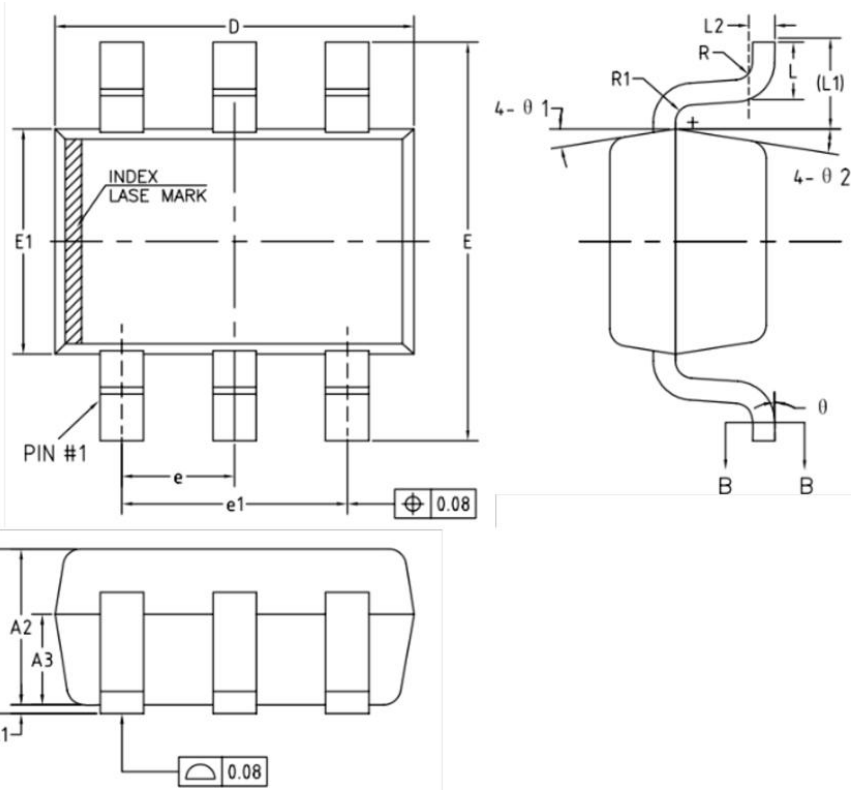
(1) Package Type: SOT23-6



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

	SYMBOL	MIN	NOM	MAX
	A	–	–	1.25
	A1	0	–	0.15
	A2	1.00	1.10	1.20
	A3	0.60	0.65	0.70
	b	0.36	–	0.50
	b1	0.36	0.38	0.45
	c	0.14	–	0.20
	c1	0.14	0.15	0.16
	D	2.826	2.926	3.026
	E	2.60	2.80	3.00
	E1	1.526	1.626	1.726
④	e	0.90	0.95	1.00
④	e1	1.80	1.90	2.00
	L	0.35	0.45	0.60
	L1	0.59REF		
	L2	0.25BSC		
③	R	0.10	–	–
③	R1	0.10	–	0.20
	θ	0°	–	8°
	θ1	3°	5°	7°
④	θ2	6°	–	14°

(2) Package Type:SC70-6



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.85	–	1.05
A1	0	–	0.10
A2	0.80	0.90	1.00
A3	0.47	0.52	0.57
2 b	0.22	–	0.29
b1	0.22	0.25	0.28
3 2 c	0.115	–	0.15
3 c1	0.115	0.13	0.14
D	2.02	2.07	2.12
E	2.20	2.30	2.40
E1	1.25	1.30	1.35
e	0.65BSC		
e1	1.30BSC		
L	0.28	0.33	0.38
L1	0.50REF		
L2	0.15BSC		
R	0.10	–	–
R1	0.10	–	0.25
θ	0°	–	8°
θ 1	6°	9°	12°
θ 2	6°	9°	12°

Important Notice And Disclaimer

- We reserves the right to change the instruction manual without prior notice.
- Any semiconductor product has a certain possibility of failure or malfunction under specific conditions. The buyer is responsible for complying with safety standards and taking safety measures when using our products for system design and overall manufacturing to avoid potential failure risks that may cause personal injury or property damage.
- The improvement of product quality is endless, our company will be dedicated to provide customers with better products.