

## Low-Power Dual Schmitt-Trigger Inverter

### Description

This dual Schmitt-trigger inverter is designed for 0.8-V to 3.6-V VCC operation.

The FLG74AUP2G14 device contains two inverters and performs the Boolean function  $Y = \overline{A}$ . The device functions as an independent inverter with Schmitt-trigger inputs, so the device has different input threshold levels for positive-going ( $V_{T+}$ ) which makes the device tolerant to slow or noisy input signals.

This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

### Features

- Inputs Accept Voltages 0.8V to 3.6 V
- Includes Schmitt-Trigger inputs
- Max Tpd of 6.1 ns at 3.3 V
- Low Static-Consumption, 0.5-  $\mu$  A Max  $I_{CC}$
- Low Noise Overshoot and Undershoot < 10% of  $V_{CC}$
- Ioff Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive

### Protection

- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at Input ( $V_{hys} = 250\text{mV}$  Typical 3.3V)
- 3.6V I/O Tolerant to Support Mixed-Mode Signal Operation
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

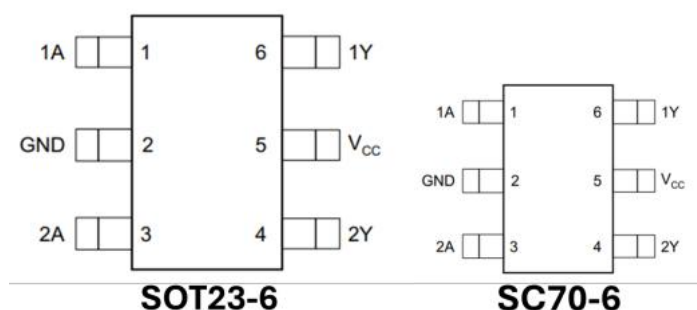
### Applications

- AV Receiver
- Smartphones
- Blu-ray Player and Home Theater
- DVD Recorders and Players
- Desktop or Notebook PCs
- Embedded PC
- GPS: Personal Navigation Devices
- Mobile Internet Devices
- Portable Media Players
- Smoke Detectors
- Solid State Drive (SSD): Enterprise
- High-Definition (HDTV)

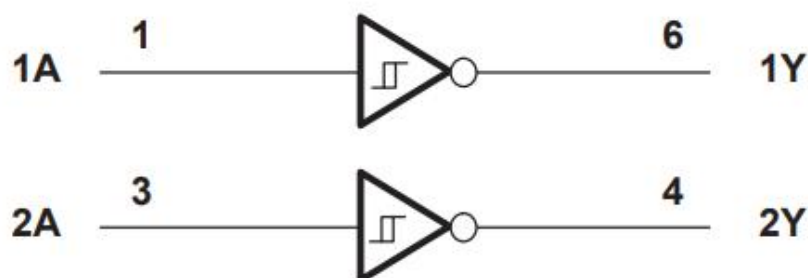
## Order information

Mode	Package	Ordering Number	Packing Option
FLG74AUP2G14	SOT-23-6	FLG74AUP2G14YSOT236G/TR	Tape and Reel,3000
	SC70-6	FLG74AUP2G14YSC706G/TR	Tape and Reel,3000

## Pin Configuration



## Simplified Schematic



## Pin Assignment

Pin Name	Pin No.	Pin Function
GND	2	Ground
1A	1	Input 1
2A	3	Input 2
1Y	6	Open-drain output 1
2Y	4	Open-drain output 2
VCC	5	Power pin

## Absolute Maximum Ratings (Note1)

- $V_{CC}$  ----- -0.5V to +4.6V
- $V_I$  ----- -0.5V to +4.6V
- $V_O$  (Voltage range applied to any output in the high-impedance or power-off state) ----- -0.3V to +4.6V
- $V_O$  (Voltage range applied to any output in the high or slow state) ----- -0.3V to  $V_{CC}+0.3V$
- Input clamp current ----- -50mA
- Output clamp current ----- -50mA
- Continuous output current -----  $\pm 20mA$
- Storage Temperature ----- -65°C to 150°C

## Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply voltage	$V_{CC}$	Operating	0.8		3.6	V
Input voltage	$V_I$		0		3.6	V
Output voltage	$V_O$		0		$V_{CC}$	V
High- level output current	$I_{OH}$	$V_{CC} = 0.8V$			-20	uA
		$V_{CC} = 1.1V$			-1.1	mA
		$V_{CC} = 1.4V$			-1.7	
		$V_{CC} = 1.65V$			-1.9	
		$V_{CC} = 2.3V$			-3.1	
		$V_{CC} = 3V$			-4	
Low- level output current	$I_{OL}$	$V_{CC} = 0.8V$			20	uA
		$V_{CC} = 1.1V$			1.1	mA
		$V_{CC} = 1.4V$			1.7	
		$V_{CC} = 1.65V$			1.9	
		$V_{CC} = 2.3V$			3.1	
		$V_{CC} = 3V$			4	
Operating temperature	$T_A$		-40		85	°C

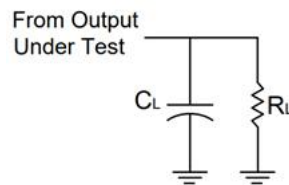
## Electrical Characteristics

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Positive-going input threshold voltage	$V_{T+}$	$V_{CC} = 0.8V$	0.3		0.6	V
		$V_{CC} = 1.1V$	0.53		0.9	
		$V_{CC} = 1.4V$	0.74		1.11	
		$V_{CC} = 1.65V$	0.91		1.29	
		$V_{CC} = 2.3V$	1.37		1.77	
		$V_{CC} = 3V$	1.88		2.29	
Negative-going input threshold voltage	$V_{T-}$	$V_{CC} = 0.8V$	0.1		0.6	V
		$V_{CC} = 1.1V$	0.26		0.65	
		$V_{CC} = 1.4V$	0.39		0.75	
		$V_{CC} = 1.65V$	0.47		0.84	
		$V_{CC} = 2.3V$	0.69		1.04	
		$V_{CC} = 3V$	0.88		1.24	
Hysteresis voltage	$\Delta V_T$	$V_{CC} = 0.8V$	0.07		0.5	V
		$V_{CC} = 1.1V$	0.08		0.46	
		$V_{CC} = 1.4V$	0.18		0.56	
		$V_{CC} = 1.65V$	0.27		0.66	
		$V_{CC} = 2.3V$	0.53		0.92	
		$V_{CC} = 3V$	0.79		1.31	
High- level output voltage	$V_{OH}$	$V_{CC} = 0.8\sim 3.6V, I_{OH} = -20\mu A$	$V_{CC}-0.1$			V
		$V_{CC} = 1.1V, I_{OH} = -1.1mA$	$0.75 \times V_{CC}$			
		$V_{CC} = 1.4V, I_{OH} = -1.7mA$	1.11			
		$V_{CC} = 1.65V, I_{OH} = -1.9mA$	1.32			
		$V_{CC} = 2.3V, I_{OH} = -2.3mA$	2.05			
		$V_{CC} = 2.3V, I_{OH} = -3.1mA$	1.9			
		$V_{CC} = 3V, I_{OH} = -2.7mA$	2.72			
		$V_{CC} = 3V, I_{OH} = -4mA$	2.6			
Low- level output voltage	$V_{OL}$	$V_{CC} = 0.8\sim 3.6V, I_{OL} = 20\mu A$			0.1	V
		$V_{CC} = 1.1V, I_{OL} = 1.1mA$			$0.3 \times V_{CC}$	
		$V_{CC} = 1.4V, I_{OL} = 1.7mA$			0.31	
		$V_{CC} = 1.65V, I_{OL} = 1.9mA$			0.31	
		$V_{CC} = 2.3V, I_{OL} = 2.3mA$			0.31	
		$V_{CC} = 2.3V, I_{OL} = 3.1mA$			0.44	
		$V_{CC} = 3V, I_{OL} = 2.7mA$			0.31	
		$V_{CC} = 3V, I_{OL} = 4mA$			0.44	
Input leakage current	$I_I$	$V_I = 3.6V$ or GND, $V_{CC} = 0\sim 3.6V$			0.1	$\mu A$
Power off leakage current	$I_{OFF}$	$V_I$ or $V_O = 0V$ to $3.6V, V_{CC} = 0V$			0.2	$\mu A$
Supply current	$I_{CC}$	$V_I = GND$ or ( $V_{CC}$ to $3.6V$ ), $I_{OUT} = 0, V_{CC} = 0.8\sim 3.6V$			0.5	$\mu A$
Additional supply current per input pin	$\Delta I_{CC}$	$V_I = V_{CC} - 0.6V, I_{OUT} = 0$			40	$\mu A$

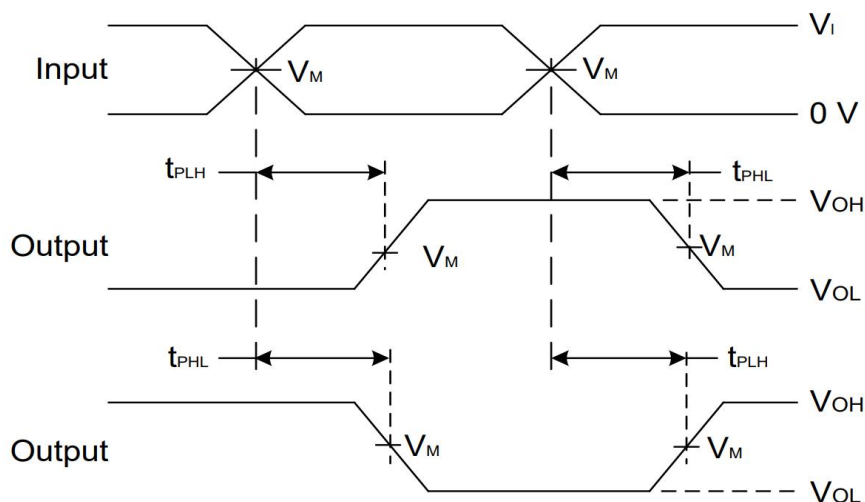
## Switching Characteristics

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Propagation delay from input(A or B) to output(Y)	$T_{PD}$	$V_{CC} = 0.8V$		20.1		ns	
		$V_{CC} = 1.2V \pm 0.1V$		5.5	8.7		14
		$V_{CC} = 1.5V \pm 0.1V$	$C_L = 15pF$	4.7	6.7		12.5
		$V_{CC} = 1.8V \pm 0.15V$	$R_L = 1M\Omega$	4.2	5.6		10.1
		$V_{CC} = 2.5V \pm 0.2V$		3.6	4.5		7.4
		$V_{CC} = 3.3V \pm 0.3V$		3.3	3.9		6.1

## Parameter Measurement Information



$V_{CC}$	INPUTS		$V_M$	$C_L$	$R_L$
	$V_I$	$t_r/t_f$			
0.8V	$V_{CC}$	$\cong 2ns$	$V_{CC}/2$	15pF	1M $\Omega$
1.2V $\pm$ 0.1V	$V_{CC}$	$\cong 2ns$	$V_{CC}/2$	15pF	1M $\Omega$
1.5V $\pm$ 0.1V	$V_{CC}$	$\cong 2ns$	$V_{CC}/2$	15pF	1M $\Omega$
1.8V $\pm$ 0.15V	$V_{CC}$	$\cong 2ns$	$V_{CC}/2$	15pF	1M $\Omega$
2.5V $\pm$ 0.2V	3V	$\cong 2.5ns$	1.5V	15pF	1M $\Omega$
3.3V $\pm$ 0.3V	$V_{CC}$	$\cong 2.5ns$	$V_{CC}/2$	15pF	1M $\Omega$



## Voltage Waveform Propagation Delay Times Inverting and Non Inverting Outputs

- Notes: A.  $C_L$  includes probe and jig capacitance  
 B. All pulses and supplied at pulse repetition rate  $\cong 10\text{MHz}$   
 C. The Inputs are measured separately one transition per measurement  
 D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{PD}$

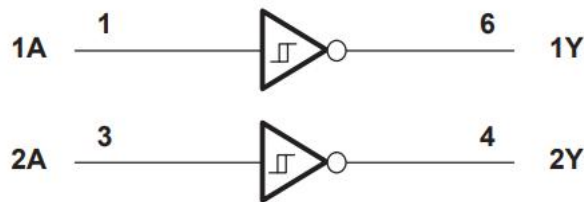
## IC Operation Information

### Basic Operation

This device functions as an independent gate with Schmitt-trigger inputs, which allows for slow input transition and better switching-noise immunity at the input.

This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered.

### Function Block Diagram



### Feature Description

- Wide operating  $V_{CC}$  range of 0.8V to 3.6V.
- 3.6-V I/O tolerant to support down translation.
- Input hysteresis allows slow input transition and better switching noise immunity at the input.
- Ioff feature allows voltages on the inputs and outputs when  $V_{CC}$  is 0 V.
- Low noise due to slower edge rates.

### Device Functional Table

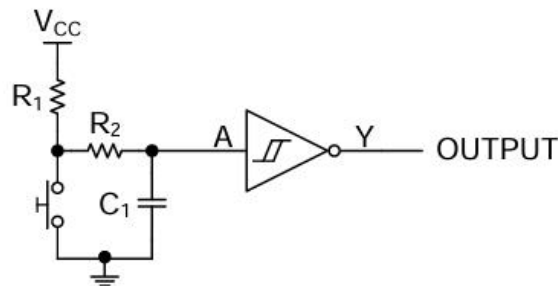
INPUTS	OUTPUT
A	Y
H	L
L	H

## IC Application Information

Mechanical input elements, such as push buttons or rotary knobs, offer simple ways to interact with electronic systems. Typically, these elements have recoil or bouncing, where the mechanical element makes and breaks contact multiple times during human interaction. This bouncing can cause one or more repeated signals to be passed, triggering multiple actions when only a single input was intended. One potential solution to mitigating these multiple inputs is by utilizing a Schmitt-trigger to create a debounce circuit. Below figure shows an example of this solution.

The input due to the push button switches multiple times, causing the output of a non-Schmitt-trigger device to trigger multiple times, while the Schmitt-trigger input device with RC delay limits the output pulse to a single pulse desired by the user. The separated positive and negative input voltage threshold values prevent multiple triggers from occurring, see the Electrical Characteristics table for  $V_{T+}$ ,  $V_{T-}$  and  $V_{hys}$  values.

## Typical Application



## Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. Drive strength also creates fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

## Detailed Design Procedure

### 1. Recommended Input conditions:

- For specified high and low levels, see ( $V_{T+}$  and  $V_{T-}$ ) in Electrical Characteristics table.
- Inputs are overvoltage tolerant allowing them to go as high as ( $V_I$  max) in the Recommended Operating Conditions table at any valid VCC.

### 2. Recommended output conditions:

- Load currents should not exceed ( $I_O$  max) per output and should not exceed (Continuous current through VCC or GND) total current for the part. These limits are located in the Absolute Maximum Ratings table.

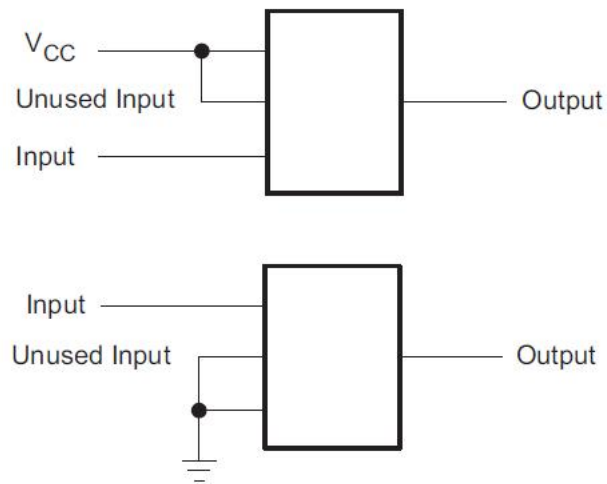
## Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the Recommended Operating Conditions table. Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu$ F is recommended; if there are multiple VCC pins, then 0.01  $\mu$ F or 0.022  $\mu$ F is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu$ F and a 1  $\mu$ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## Layout Considerations

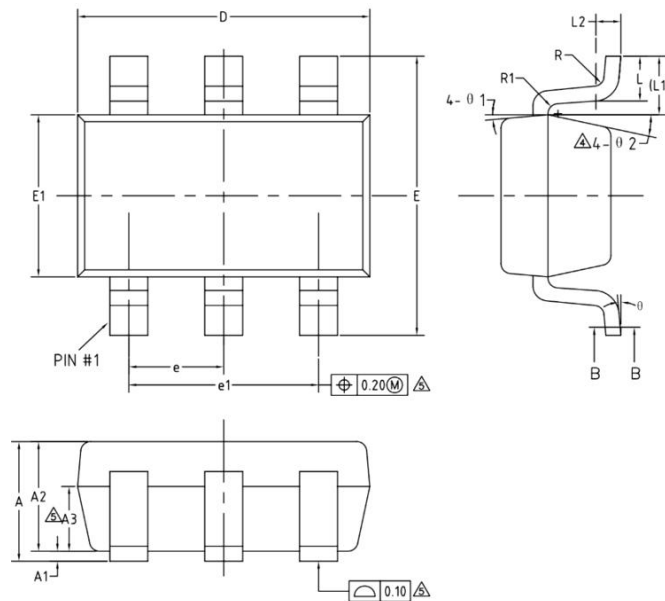
When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Below figure specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or VCC, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.



## Package Information

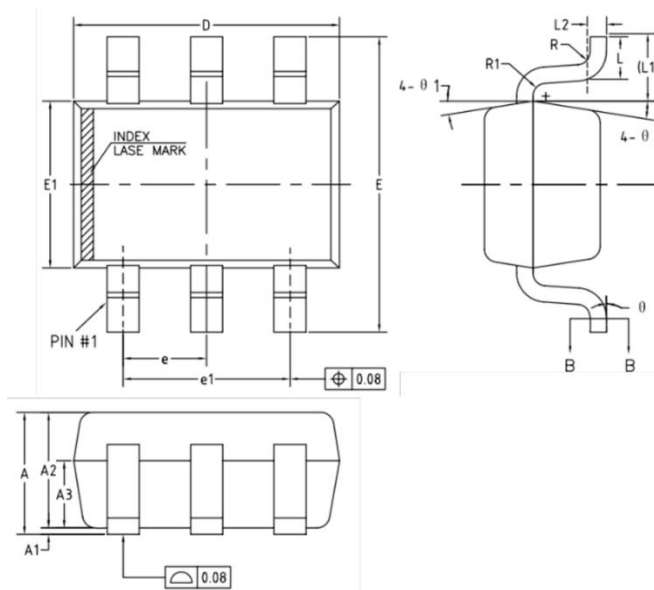
(1) Package Type: SOT23-6



COMMON DIMENSIONS  
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.25
A1	0	—	0.15
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.36	—	0.50
b1	0.36	0.38	0.45
c	0.14	—	0.20
c1	0.14	0.15	0.16
D	2.826	2.926	3.026
E	2.60	2.80	3.00
E1	1.526	1.626	1.726
$\triangle 4$ e	0.90	0.95	1.00
$\triangle 4$ e1	1.80	1.90	2.00
L	0.35	0.45	0.60
L1	0.59REF		
L2	0.25BSC		
$\triangle 3$ R	0.10	—	—
$\triangle 3$ R1	0.10	—	0.20
$\theta$	0°	—	8°
$\theta 1$	3°	5°	7°
$\triangle 4$ $\theta 2$	6°	—	14°

(2) Package Type:SC70-6



COMMON DIMENSIONS  
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.85	—	1.05
A1	0	—	0.10
A2	0.80	0.90	1.00
A3	0.47	0.52	0.57
b	0.22	—	0.29
b1	0.22	0.25	0.28
c	0.115	—	0.15
c1	0.115	0.13	0.14
D	2.02	2.07	2.12
E	2.20	2.30	2.40
E1	1.25	1.30	1.35
e	0.65BSC		
e1	1.30BSC		
L	0.28	0.33	0.38
L1	0.50REF		
L2	0.15BSC		
R	0.10	—	—
R1	0.10	—	0.25
θ	0°	—	8°
θ 1	6°	9°	12°
θ 2	6°	9°	12°

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- We reserves the right to change the instruction manual without prior notice.
- Any semiconductor product has a certain possibility of failure or malfunction under specific conditions. The buyer is responsible for complying with safety standards and taking safety measures when using our products for system design and overall manufacturing to avoid potential failure risks that may cause personal injury or property damage.
- The improvement of product quality is endless, our company will be dedicated to provide customers with better products.