

## Quadruple Bus Buffer Gate With 3-State Output

### Description

The quadruple buffer is designed for 1.65-V to 5.5-V VCC operation.

The FLG74LVC126A device is a single line driver with a 3-state output. Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times. The output is disabled when the output-enable input is low.

The FLG74LVC126A is available in a variety of packages, including the SO14/TSSOP14 package with a body size of 8.65mmX6mm & 5mm ×4.4mm.

### Features

- Supports 5-V VCC Operation
- Inputs Accept Voltages 1.65V to 5.5 V
- Low Power Consumption, 10-  $\mu$  A Max  $I_{CC}$
- $\pm 24$ -mA Output Drive at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.8V at  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$

- Typical  $V_{OHV}$  (Output VOH Undershoot) > 2V at  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

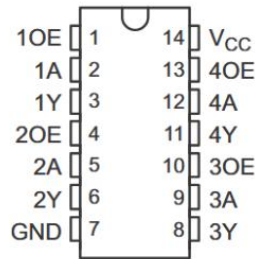
### Applications

- Cable Modem Termination System
- High-Speed Data Acquisition and Generation
- Military: Radar and Sonar
- Motor Control: High-Voltage
- Power Line Communication Modem
- SSD: Internal or External
- Video Broadcasting and Infrastructure: Scalable Platform
- Video Broadcasting: IP-Based Multi-Format Transcoder
- Video Communications System

## Order information

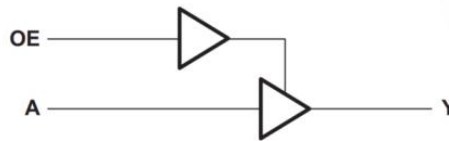
Mode	Package	Ordering Number	Packing Option
FLG74LVC126A	SOP14	FLG74LVC126AYSOP14G/TR	Tape and Reel,2500
	TSSOP14	FLG74LVC126AYTSSOP14G/TR	Tape and Reel,2500

## Pin Configuration



SO14 / TSSOP14

## Simplified Schematic



Logic Diagram, Each Gate  
(Positive Logic)

## Pin Assignment

Pin Name	Pin No.	Pin No.	Pin Function
1OE	1	I	Output Enable 1
1A	2	I	Channel 1 input A
1Y	3	O	Channel 1 output
2OE	4	I	Output Enable 2
2A	5	I	Channel 2 input A
2Y	6	O	Channel 2 output
GND	7	Ground	Ground
3Y	8	O	Channel 3 output
3A	9	I	Channel 3 input A
3OE	10	I	Output Enable 3
4Y	11	O	Channel 4 output
4A	12	I	Channel 4 input A
4OE	13	I	Output Enable 4
VCC	14	Power	Positive Supply

## Absolute Maximum Ratings (Note1)

- $V_{CC}$  ----- -0.5V to +6.5V
- $V_I$  ----- -0.5V to +6.5V
- $V_O$  (Voltage range applied to any output in the high-impedance or power-off state) ----- -0.5V to  $V_{CC}+0.5V$
- $V_O$  (Voltage range applied to any output in the high or slow state) ----- -0.5V to  $V_{CC}+0.5V$
- Input clamp current ----- -50mA
- Output clamp current ----- -50mA
- Continuous output current -----  $\pm 50mA$
- Storage Temperature -----  $-65^{\circ}C$  to  $150^{\circ}C$

## Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply voltage	$V_{CC}$	Operating	1.65		5.5	V
		Data retention only	1.5			
Input voltage	$V_I$		0		5.5	V
Output voltage	$V_O$				$V_{CC}$	V
High- level input voltage	$V_{IH}$	$V_{CC} = 1.65V$ to $1.95V$	$0.65 \times V_{CC}$			V
		$V_{CC} = 2.3V$ to $2.7V$	1.7			
		$V_{CC} = 3V$ to $3.6V$	2			
		$V_{CC} = 4.5V$ to $5.5V$	$0.7 \times V_{CC}$			
Low- level input voltage	$V_{IL}$	$V_{CC} = 1.65V$ to $1.95V$			$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3V$ to $2.7V$			0.7	
		$V_{CC} = 3V$ to $3.6V$			0.8	
		$V_{CC} = 4.5V$ to $5.5V$			$0.3 \times V_{CC}$	
High- level output current	$I_{OH}$	$V_{CC} = 1.65V$			-4	mA
		$V_{CC} = 2.3V$			-8	
		$V_{CC} = 3V$			-16	
		$V_{CC} = 3V$			-24	
		$V_{CC} = 4.5V$			-32	
Low- level output current	$I_{OL}$	$V_{CC} = 1.65V$			4	mA
		$V_{CC} = 2.3V$			8	
		$V_{CC} = 3V$			16	
		$V_{CC} = 3V$			24	
		$V_{CC} = 4.5V$			32	
Input transition rise or fall rate	$\Delta T/\Delta V$	$V_{CC} = 1.8V \pm 0.15V, 2.5V \pm 0.2V$			20	ns/V
		$V_{CC} = 3.3V \pm 0.3V$			10	
		$V_{CC} = 5V \pm 0.5V$			5	
Operating temperature	$T_A$		-40		125	$^{\circ}C$

## Electrical Characteristics

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
High- level output voltage	$V_{OH}$	$V_{CC} = 1.65\sim 5.5V, I_{OH} = 100\mu A$	$V_{CC}-0.1$			V
		$V_{CC} = 1.65V, I_{OH} = 4mA$	1.2			
		$V_{CC} = 2.3V, I_{OH} = 8mA$	1.9			
		$V_{CC} = 3V, I_{OH} = 16mA$	2.4			
		$V_{CC} = 3V, I_{OH} = 24mA$	2.3			
		$V_{CC} = 4.5V, I_{OH} = 32mA$	3.8			
Low- level output voltage	$V_{OL}$	$V_{CC} = 1.65\sim 5.5V, I_{OL} = 100\mu A$			0.1	V
		$V_{CC} = 1.65V, I_{OL} = 4mA$			0.45	
		$V_{CC} = 2.3V, I_{OL} = 8mA$			0.3	
		$V_{CC} = 3V, I_{OL} = 16mA$			0.4	
		$V_{CC} = 3V, I_{OL} = 24mA$			0.55	
		$V_{CC} = 4.5V, I_{OL} = 32mA$			0.55	
Input leakage current	$I_I$	$V_{IN} = 5.5V$ or GND, $V_{CC} = 0\sim 5.5V$			$\pm 5$	$\mu A$
Power off leakage current	$I_{OFF}$	$V_I$ or $V_O = 5.5V, V_{CC} = 0V$			$\pm 10$	$\mu A$
Supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0, V_{CC} = 1.65\sim 5.5V$			10	$\mu A$
Additional supply current per input pin	$\Delta I_{CC}$	$V_{CC} = 3\sim 5.5V$ , one input at $V_{CC} - 0.6V$ , other input at $V_{CC}$ or GND			500	$\mu A$

## Switching Characteristics

Parameter	From Input	To Output	Test Conditions	Min.	Typ.	Max.	Unit
$T_{PD}$	A	Y	$V_{CC} = 1.8V \pm 0.15V$	2.6		8	ns
			$V_{CC} = 2.5V \pm 0.2V$	1.1		5.5	
			$V_{CC} = 3.3V \pm 0.3V$	1		4.5	
			$V_{CC} = 5V \pm 0.5V$	1		4	
$T_{en}$	OE	Y	$V_{CC} = 1.8V \pm 0.15V$	2.8		9.4	ns
			$V_{CC} = 2.5V \pm 0.2V$	1.3		6.6	
			$V_{CC} = 3.3V \pm 0.3V$	1.2		5.3	
			$V_{CC} = 5V \pm 0.5V$	1		5	
$T_{dis}$	OE	Y	$V_{CC} = 1.8V \pm 0.15V$	1.6		9.8	ns
			$V_{CC} = 2.5V \pm 0.2V$	1		5.5	
			$V_{CC} = 3.3V \pm 0.3V$	1		5.5	
			$V_{CC} = 5V \pm 0.5V$	1		4.2	

## Typical Characteristics

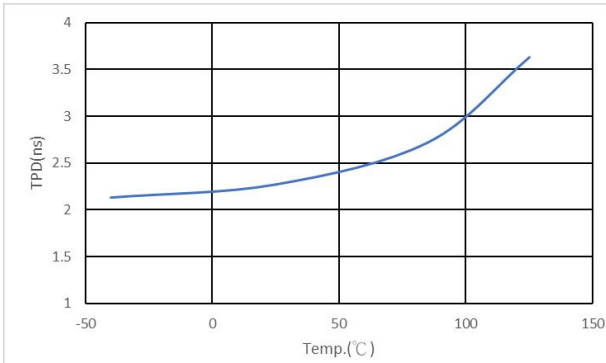


Fig.1 TPD across Temperature at 3.3V VCC

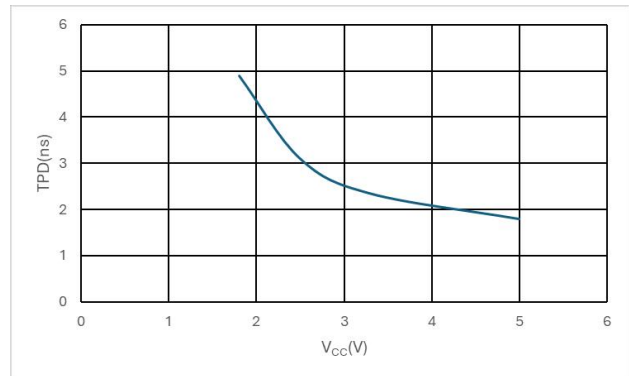
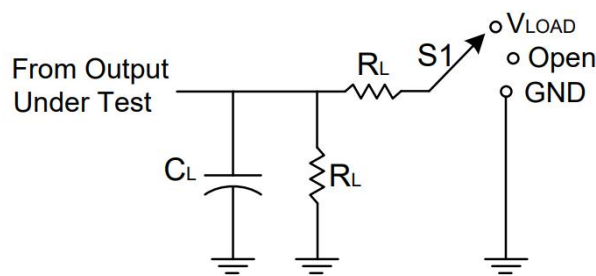


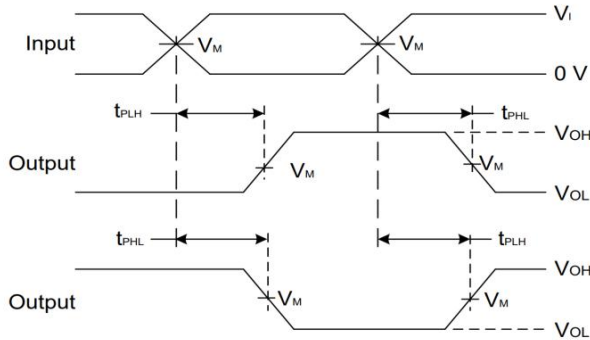
Fig.2 TPD across VCC at 25°C

## Parameter Measurement Information

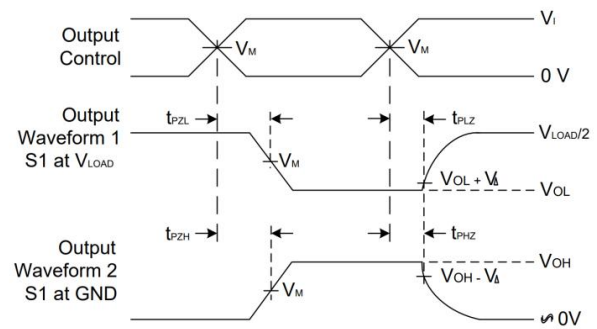


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8V \pm 0.15V$	$V_{CC}$	$\cong 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	30pF	1k $\Omega$	0.15V
$2.5V \pm 0.2V$	$V_{CC}$	$\cong 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	30pF	500 $\Omega$	0.15V
$3.3V \pm 0.3V$	3V	$\cong 2.5ns$	1.5V	6V	50pF	500 $\Omega$	0.3V
$5V \pm 0.5V$	$V_{CC}$	$\cong 2.5ns$	$V_{CC}/2$	$2 \times V_{CC}$	50pF	500 $\Omega$	0.3V



Voltage Waveform Propagation Delay Times  
Inverting and Non Inverting Outputs



Voltage Waveform Enable and Disable Times  
Low- and High-Level Enabling

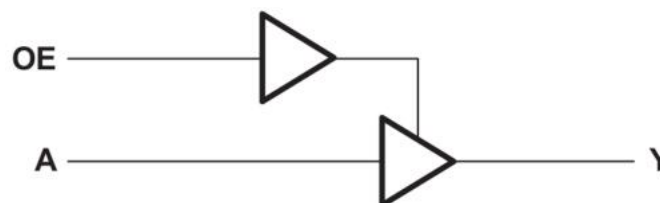
- Notes:
- A.  $C_L$  includes probe and jig capacitance
  - B. All pulses and supplied at pulse repetition rate  $\cong 10\text{MHz}$
  - C. The Inputs are measured separately one transition per measurement
  - D.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$
  - E.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$
  - F.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{PD}$

## IC Operation Information

### Basic Operation

The FLG74LVC126A device contains four buffer gate device with output enable control and performs the Boolean function  $Y = A \cdot OE$ . This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. To ensure the high-impedance state during power up or power down, OE should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### Function Block Diagram



## Feature Description

- Wide operating voltage range.
  - Operates from 1.65 V to 5.5 V.
- Allows down voltage translation.
- Inputs accept voltages to 5.5 V.
- Ioff feature allows voltages on the inputs and outputs when  $V_{CC}$  is 0 V.

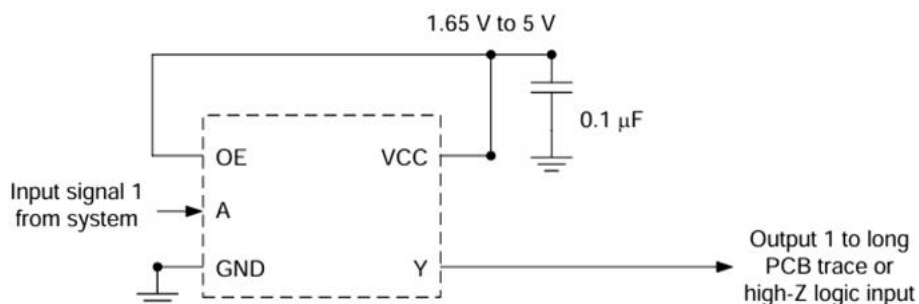
## Device Functional Table

INPUTS		OUTPUT Y
$\overline{O E}$	A	
L	H	H
L	L	L
H	X	Z

## IC Application Information

The FLG74LVC126A is a high drive CMOS device that can be used as an output enabled buffer with a high output drive, such as an LED application. It can produce 24 mA of drive current at 3.3 V, making it ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5 V tolerant allowing it to translate down to  $V_{CC}$ .

## Typical Application



## Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

## Detailed Design Procedure

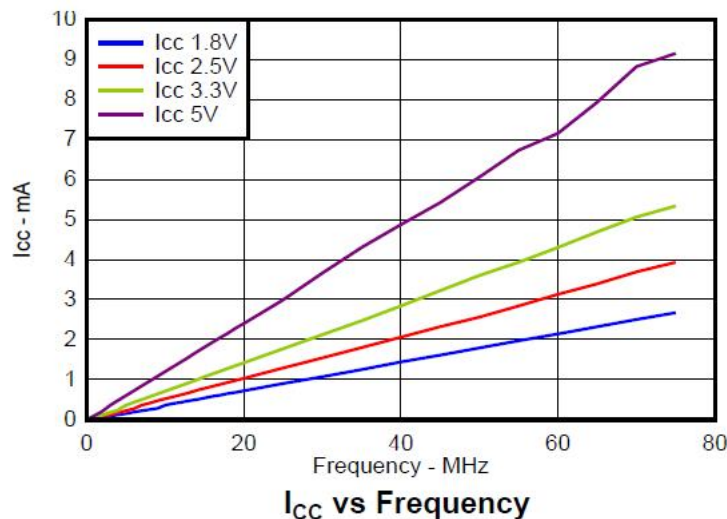
### 1. Recommended Input Conditions

- Rise time and fall time specs. See ( $\Delta t / \Delta V$ ) in the Recommended Operating Conditions table.
- Specified high and low levels. See ( $V_{IH}$  and  $V_{IL}$ ) in the Recommended Operating Conditions table
- Inputs are overvoltage tolerant allowing them to go as high as ( $V_I \max$ ) in the Recommended Operating Conditions table at any valid  $V_{CC}$ .

### 2. Recommend Output Conditions

- Load currents should not exceed ( $I_O \max$ ) per output and should not exceed total current (continuous current through  $V_{CC}$  or GND) for the part. These limits are located in the Absolute Maximum Ratings table.
- Outputs should not be pulled above  $V_{CC}$ .

## Application Curves



## Power Supply Recommendations

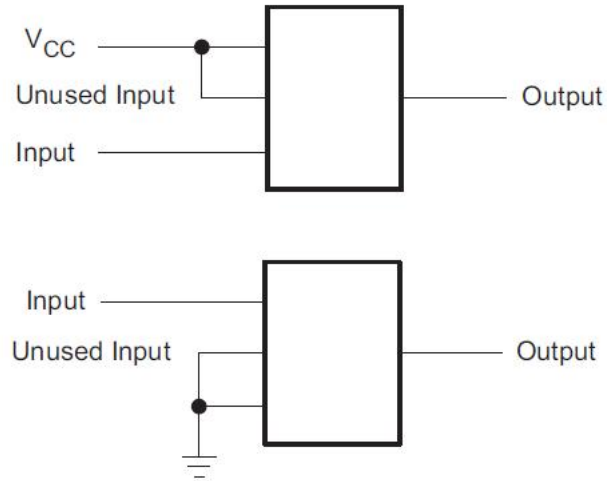
The power supply can be any voltage between the min and max supply voltage rating located in the Recommended Operating Conditions table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- $\mu\text{F}$  capacitor is recommended and if there are multiple  $V_{CC}$  pins then 0.01- $\mu\text{F}$  or 0.022- $\mu\text{F}$  capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- $\mu\text{F}$  and 1- $\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## Layout Considerations

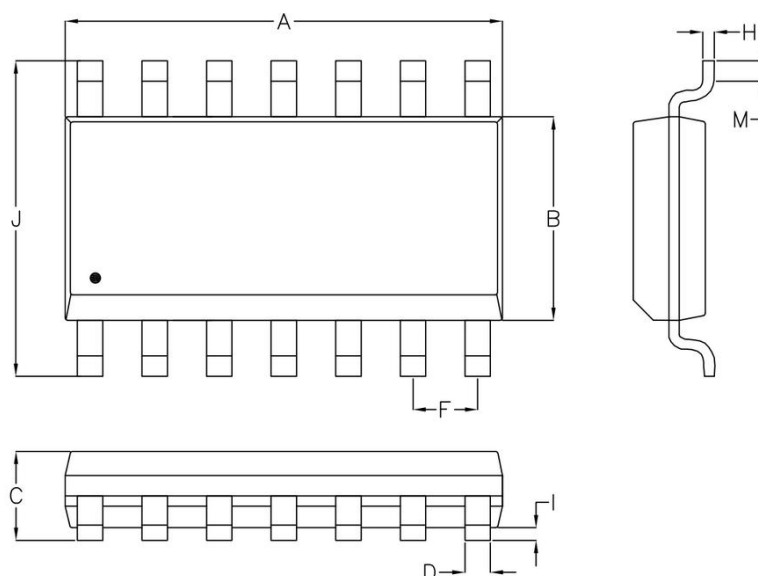
When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input Exclusive-OR gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the

outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or VCC whichever make more sense or is more convenient.



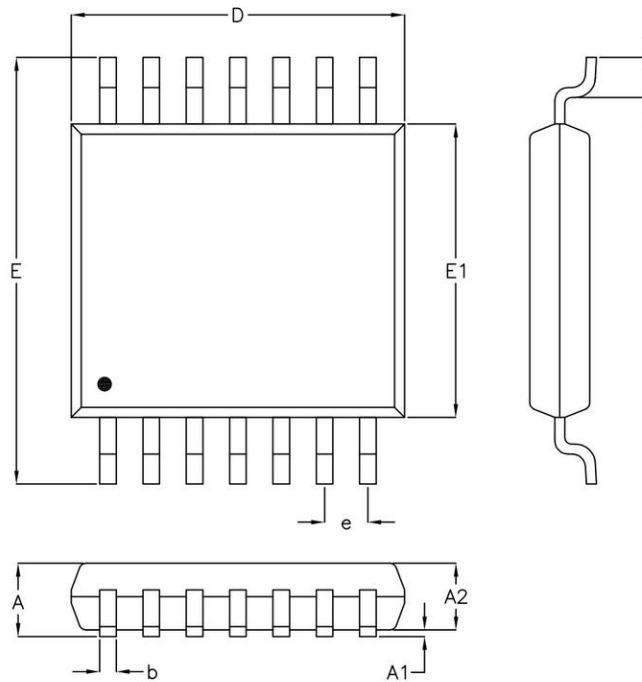
## Package Information

(1) Package Type: SO14



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	8.534	8.738	0.336	0.344
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050

(2) Package Type: TSSOP14



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.000	1.200	0.039	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
D	4.900	5.100	0.193	0.201
e	0.650		0.026	
E	6.300	6.500	0.248	0.256
E1	4.300	4.500	0.169	0.177
L	0.450	0.750	0.018	0.030

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