

## Hex Schmitt-Trigger Inverter

### Description

This hex Schmitt-trigger inverter is designed for 1.65-V to 5.5-V VCC operation.

The FLG74LVC14A device contains six inverter and performs the Boolean function  $Y = \bar{A}$ . The device functions as an independent inverter with Schmitt-trigger inputs, so the device has different input threshold levels for positive-going  $V_{T+}$  which makes the device tolerant to slow or noisy input signals.

### Features

- Inputs Accept Voltages 1.65V to 5.5 V
- Max Tpd of 6.4 ns at 3.3 V
- Low Power Consumption, 10-  $\mu$  A Max  $I_{CC}$
- $\pm 24$ -mA Output Drive at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8V at  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$
- Typical  $V_{OHV}$  (Output VOH Undershoot) > 2V at  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

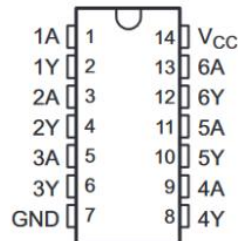
### Applications

- AV Receiver
- Audio Dock: Portable
- Blu-ray Player and Home Theater
- Embedded PC
- Personal Digital Assistant (PDA)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid State Drive (SSD): Client and Enterprise
- TVs: LCD/Digital and High-Definition (HDTV)
- Tablet: Enterprise
- Video Analytics: Server
- Wireless Headset, Keyboard, and Mouse

## Order information

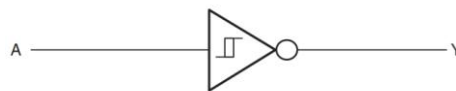
Mode	Package	Ordering Number	Packing Option
FLG74LVC14A	SO14	FLG74LVC14AYSOP14G/TR	Tape and Reel,2500
	TSSOP14	FLG74LVC14AYTSSOP14G/TR	Tape and Reel,2500

## Pin Configuration



SO14 / TSSOP14

## Simplified Schematic



Logic Diagram, Each Gate  
(Positive Logic)

## Pin Assignment

Pin Name	Pin No.	Pin No.	Pin Function
1A	1	I	Channel 1 Data Input
1Y	2	O	Channel 1 Data Output
2A	3	I	Channel 2 Data Input
2Y	4	O	Channel 2 Data Output
3A	5	I	Channel 3 Data Input
3Y	6	O	Channel 3 Data Output
GND	7	Ground	Ground
4A	8	I	Channel 4 Data Input
4Y	9	I	Channel 4 Data Output
5A	10	O	Channel 5 Data Input
5Y	11	I	Channel 5 Data Output
6A	12	I	Channel 6 Data Input
6Y	13	O	Channel 6 Data Output
VCC	14	Power	Positive Supply

## Absolute Maximum Ratings (Note1)

- $V_{CC}$  ----- -0.5V to + 6.5V
- $V_I$  ----- - 0.5V to + 6.5V
- $V_O$  (Voltage range applied to any output in the high-impedance or power-off state) ----- - 0.5V to + 6.5V
- $V_O$ (Voltage range applied to any output in the high or slow state )----- -0.5V to  $V_{CC}+0.5V$
- Input clamp current ----- -50mA
- Output clamp current ----- -50mA
- Continuous output current -----  $\pm 50mA$
- Storage Temperature -----  $-65^{\circ}C$  to  $150^{\circ}C$

## Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply voltage	$V_{CC}$	Operating	1.65		5.5	V
Input voltage	$V_I$		0		5.5	V
Output voltage	$V_O$				$V_{CC}$	V
High- level output current	$I_{OH}$	$V_{CC} = 1.65V$			-4	mA
		$V_{CC} = 2.3V$			-8	
		$V_{CC} = 3V$			-16	
		$V_{CC} = 3V$			-24	
		$V_{CC} = 4.5V$			-32	
Low- level output current	$I_{OL}$	$V_{CC} = 1.65V$			4	mA
		$V_{CC} = 2.3V$			8	
		$V_{CC} = 3V$			16	
		$V_{CC} = 3V$			24	
		$V_{CC} = 4.5V$			32	
Operating temperature	$T_A$		-40		125	$^{\circ}C$

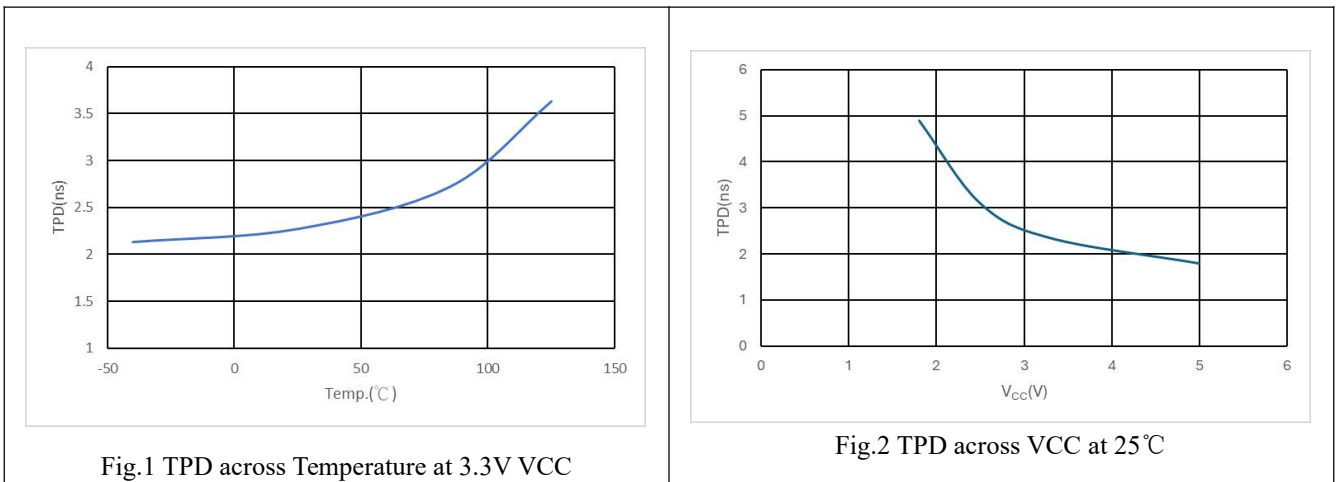
## Electrical Characteristics

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Positive-going input threshold voltage	$V_{T+}$	$V_{CC} = 1.65V$	0.79		1.16	V
		$V_{CC} = 2.3V$	1.11		1.56	
		$V_{CC} = 3V$	1.5		1.87	
		$V_{CC} = 4.5V$	2.16		2.74	
		$V_{CC} = 5.5V$	2.61		3.33	
Negative-going input threshold voltage	$V_{T-}$	$V_{CC} = 1.65V$	0.39		0.62	V
		$V_{CC} = 2.3V$	0.58		0.87	
		$V_{CC} = 3V$	0.84		1.14	
		$V_{CC} = 4.5V$	1.41		1.79	
		$V_{CC} = 5.5V$	1.87		2.29	
Hysteresis voltage	$\Delta VT$	$V_{CC} = 1.65V$	0.37		0.62	V
		$V_{CC} = 2.3V$	0.48		0.77	
		$V_{CC} = 3V$	0.56		0.87	
		$V_{CC} = 4.5V$	0.71		1.04	
		$V_{CC} = 5.5V$	0.71		1.11	
High- level output voltage	$V_{OH}$	$V_{CC} = 1.65\sim 5.5V, I_{OH}= 100\mu A$	$V_{CC}-0.1$			V
		$V_{CC} = 1.65V, I_{OH}= 4mA$	1.2			
		$V_{CC} = 2.3V, I_{OH}= 8mA$	1.9			
		$V_{CC} = 3V, I_{OH}= 16mA$	2.4			
		$V_{CC} = 3V, I_{OH}= 24mA$	2.3			
		$V_{CC} = 4.5V, I_{OH}= 32mA$	3.8			
Low- level output voltage	$V_{OL}$	$V_{CC} = 1.65\sim 5.5V, I_{OL}= 100\mu A$			0.1	V
		$V_{CC} = 1.65V, I_{OL}= 4mA$			0.45	
		$V_{CC} = 2.3V, I_{OL}= 8mA$			0.3	
		$V_{CC} = 3V, I_{OL}= 16mA$			0.4	
		$V_{CC} = 3V, I_{OL}= 24mA$			0.55	
		$V_{CC} = 4.5V, I_{OL}= 32mA$			0.55	
Input leakage current	$I_I$	$V_{IN}= 5.5V$ or GND, $V_{CC}= 0\sim 5.5V$			$\pm 5$	$\mu A$
Power off leakage current	$I_{OFF}$	$V_I$ or $V_O=5.5V, V_{CC}=0V$			$\pm 10$	$\mu A$
Supply current	$I_{CC}$	$V_{IN}= V_{CC}$ or GND , $I_{OUT}=0, V_{CC}= 1.65\sim 5.5V$			10	$\mu A$
Additional supply current per input pin	$\Delta I_{CC}$	$V_{CC}=3\sim 5.5V$ , one input at $V_{CC}-0.6V$ , other input at $V_{CC}$ or GND			500	$\mu A$

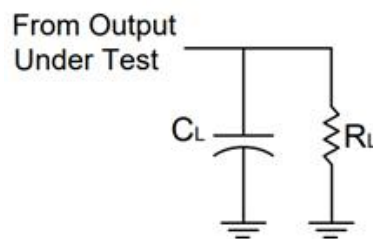
## Switching Characteristics

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Propagation delay from input(A ) to output(Y)	T <sub>PD</sub>	V <sub>CC</sub> = 1.8V±0.15V	1		10.5	ns
		V <sub>CC</sub> = 2.5V±0.2V	1		7.3	
		V <sub>CC</sub> = 3.3V±0.3V	1		6.2	
		V <sub>CC</sub> = 5V±0.5V	1		6.2	

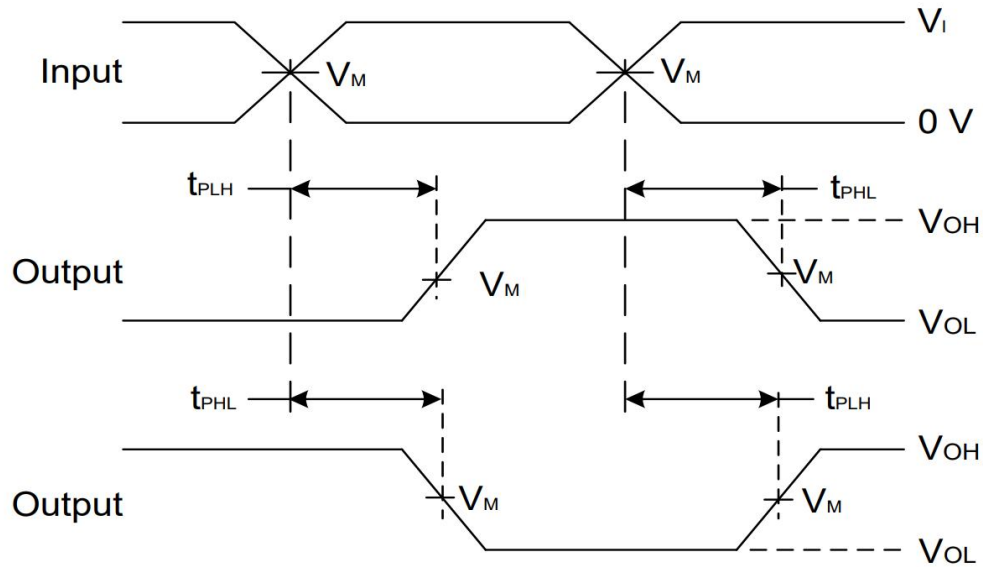
## Typical Characteristics



## Parameter Measurement Information



V <sub>CC</sub>	INPUTS		V <sub>M</sub>	C <sub>L</sub>	R <sub>L</sub>
	V <sub>I</sub>	t <sub>r</sub> /t <sub>f</sub>			
1.8V ± 0.15V	V <sub>CC</sub>	≅ 2ns	V <sub>CC</sub> /2	15pF	1MΩ
2.5V ± 0.2V	V <sub>CC</sub>	≅ 2ns	V <sub>CC</sub> /2	15pF	1MΩ
3.3V ± 0.3V	3V	≅ 2.5ns	1.5V	15pF	1MΩ
5V ± 0.5V	V <sub>CC</sub>	≅ 2.5ns	V <sub>CC</sub> /2	15pF	1MΩ



Voltage Waveform Propagation Delay Times

Inverting and Non Inverting Outputs

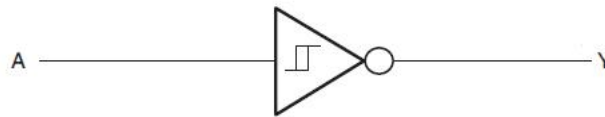
- Notes:
- A.  $C_L$  includes probe and jig capacitance
  - B. All pulses and supplied at pulse repetition rate  $\cong 10\text{MHz}$
  - C. The Inputs are measured separately one transition per measurement
  - D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{PD}$

## IC Operation Information

### Basic Operation

The FLG74LVC14A hex Schmitt-trigger inverter is designed for 1.65 V to 5.5 V operation and performs the Boolean function  $Y=\overline{A}$ . This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The SO14/TSSOP14 package technology is a major breakthrough in IC packaging.

### Function Block Diagram



### Feature Description

- Wide operating voltage range.
  - Operates from 1.65 V to 5.5 V.
- Allows down voltage translation.
- Inputs accept voltages to 5.5 V.
- Ioff feature allows voltages on the inputs and outputs when  $V_{CC}$  is 0 V.

### Device Functional Table

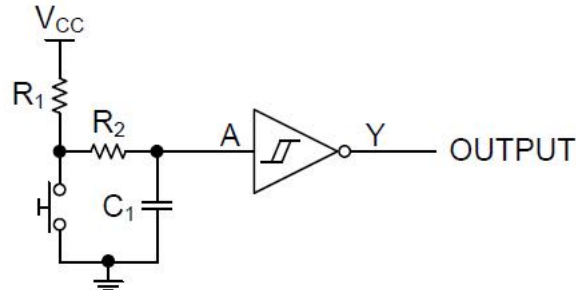
INPUTS	OUTPUT
A	Y
H	L
L	H

### IC Application Information

Mechanical input elements, such as push buttons or rotary knobs, offer simple ways to interact with electronic systems. Typically, these elements have recoil or bouncing, where the mechanical element makes and breaks contact multiple times during human interaction. This bouncing can cause one or more repeated signals to be passed, triggering multiple actions when only a single input was intended. One potential solution to mitigating these multiple inputs is by utilizing a Schmitt-trigger to create a debounce circuit.

## Typical Application

The input due to the push button switches multiple times, causing the output of a non Schmitt-trigger device to trigger multiple times, while the Schmitt-trigger input device with RC delay limits the output pulse to a single pulse desired by the user. The separated positive and negative input voltage threshold values, see Figure , prevent multiple triggers from occurring.



**Push Button Debounce Circuit Schematic**

## Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

## Detailed Design Procedure

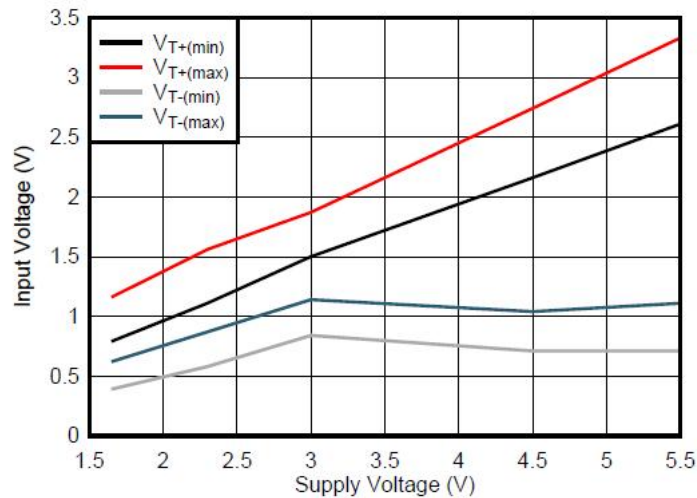
### 1. Recommended Input Conditions

- Rise time and fall time specs. See ( $\Delta t / \Delta V$ ) in the Recommended Operating Conditions table.
- Specified high and low levels. See ( $V_{IH}$  and  $V_{IL}$ ) in the Recommended Operating Conditions table.
- Inputs are overvoltage tolerant allowing them to go as high as ( $V_I \text{ max}$ ) in the Recommended Operating Conditions table at any valid  $V_{CC}$ .

### 2. Recommend Output Conditions

- Load currents should not exceed ( $I_O \text{ max}$ ) per output and should not exceed total current (continuous current through  $V_{CC}$  or GND) for the part. These limits are located in the Absolute Maximum Ratings table
- Outputs should not be pulled above  $V_{CC}$ .

## Application Curves



Interpolated Threshold Voltages vs.  $V_{CC}$

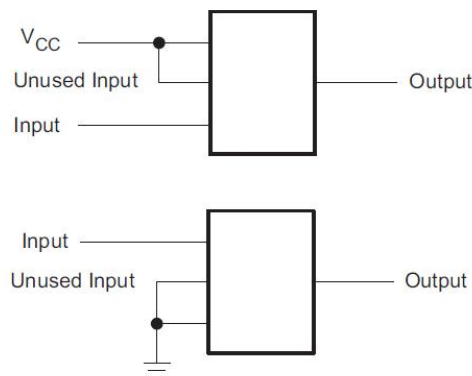
## Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the Recommended Operating Conditions table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- $\mu\text{F}$  capacitor is recommended and if there are multiple  $V_{CC}$  pins then 0.01- $\mu\text{F}$  or 0.022- $\mu\text{F}$  capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- $\mu\text{F}$  and 1- $\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

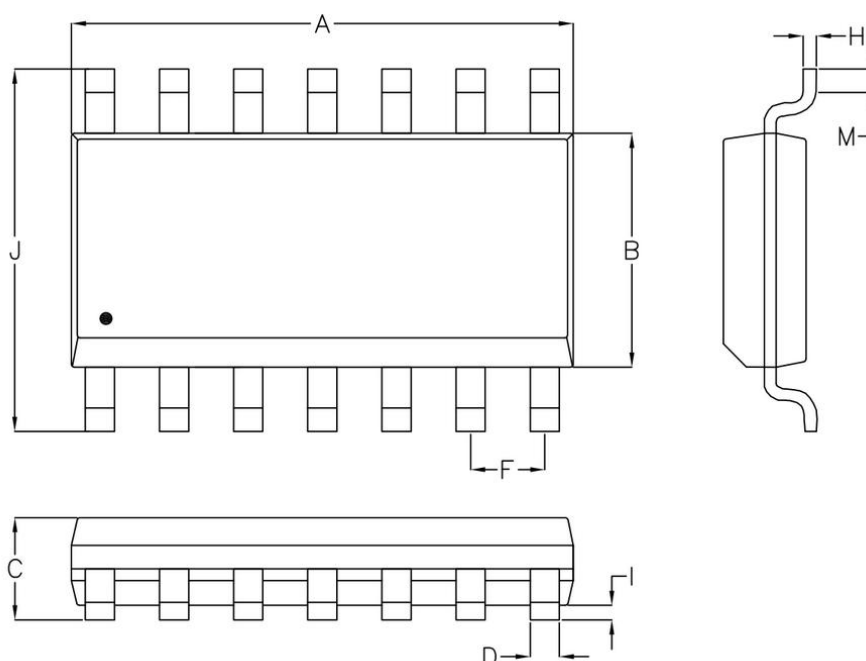
## Layout Considerations

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input buffer gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$  whichever make more sense or is more convenient.



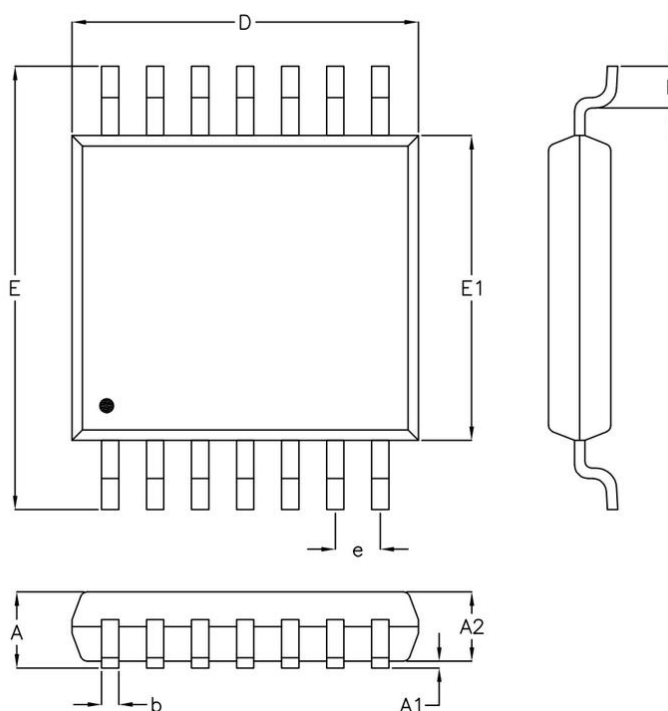
## Package Information

(1) Package Type:SO14



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	8.534	8.738	0.336	0.344
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050

(2) Package Type:TSSOP14



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.000	1.200	0.039	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
D	4.900	5.100	0.193	0.201
e	0.650		0.026	
E	6.300	6.500	0.248	0.256
E1	4.300	4.500	0.169	0.177
L	0.450	0.750	0.018	0.030

## Important Notice And Disclaimer

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- Any semiconductor product has a certain possibility of failure or malfunction under specific conditions. The buyer is responsible for complying with safety standards and taking safety measures when using our products for system design and overall manufacturing to avoid potential failure risks that may cause personal injury or property damage.
- The improvement of product quality is endless, our company will be dedicated to provide customers with better products.