

## 2-Input Positive-AND Gate

### Description

This single 2-input positive-AND gate is designed for 1.65-V to 5.5-V VCC operation. The CMOS device provides high output drive while maintaining low static power consumption.

The FLG74LVC1G08 device performs the

Boolean function  $Y = A \cdot B$  or  $Y = \overline{\overline{A} + \overline{B}}$  in positive logic. Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

The FLG74LVC1G08 is available in a variety of packages, including SOT-23-5, SC70.

### Features

- Inputs Accept Voltages 1.65V to 5.5 V
- Max Tpd of 3.6 ns at 3.3 V
- Low Power Consumption, 10-  $\mu$  A Max  $I_{CC}$
- $\pm 24$ -mA Output Drive at 3.3 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

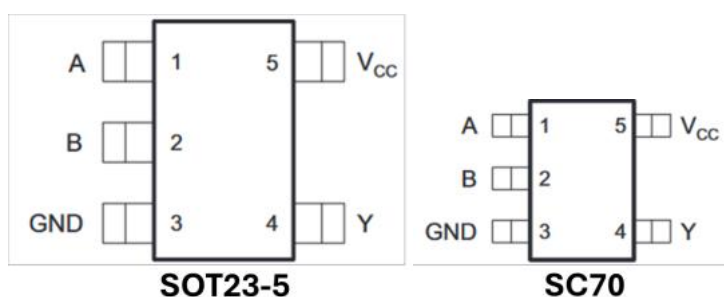
### Applications

- Active Noise Cancellation (ANC)
- DLP 3D Machine Vision, Hyperspectral Imaging, Optical Networking, and Spectroscopy
- Embedded PC
- Fingerprint Biometrics
- HVAC: Heating, Ventilating, and Air Conditioning
- Network-Attached Storage (NAS)
- Server Motherboard and PSU
- Software Defined Radio (SDR)
- TV: High-Definition (HDTV), LCD, and Digital Video Communications System
- Wireless Data Access Card, Headset, Keyboard, Mouse, and LAN Card

## Order information

Mode	Package	Ordering Number	Packing Option
FLG74LVC1G08	SOT23-5	FLG74LVC1G08YSOT235G/TR	Tape and Reel,3000
	SC70	FLG74LVC1G08YSC70G/TR	Tape and Reel,3000

## Pin Configuration



## Simplified Schematic



## Pin Assignment

Pin Name	Pin No.	Pin Function
A	1	Input
B	2	Input
GND	3	Ground
Y	4	Output
VCC	5	Power Pin

## Absolute Maximum Ratings (Note1)

- $V_{CC}$  ----- -0.5V to +6.5V
- $V_I$  ----- -0.5V to +6.5V
- $V_O$  (Voltage range applied to any output in the high-impedance or power-off state) ----- -0.5V to +6.5V
- $V_O$  (Voltage range applied to any output in the high or slow state) ----- -0.5V to  $V_{CC}+0.5V$
- Input clamp current ----- -50mA
- Output clamp current ----- -50mA
- Continuous output current -----  $\pm 50mA$
- Storage Temperature -----  $-65^{\circ}C$  to  $150^{\circ}C$

## Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply voltage	$V_{CC}$	Operating	1.65		5.5	V
		Data retention only	1.5			
Input voltage	$V_I$		0		5.5	V
Output voltage	$V_O$				$V_{CC}$	V
High- level input voltage	$V_{IH}$	$V_{CC} = 1.65V$ to $1.95V$	$0.65 \times V_{CC}$			V
		$V_{CC} = 2.3V$ to $2.7V$	1.7			
		$V_{CC} = 3V$ to $3.6V$	2			
		$V_{CC} = 4.5V$ to $5.5V$	$0.7 \times V_{CC}$			
Low- level input voltage	$V_{IL}$	$V_{CC} = 1.65V$ to $1.95V$			$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3V$ to $2.7V$			0.7	
		$V_{CC} = 3V$ to $3.6V$			0.8	
		$V_{CC} = 4.5V$ to $5.5V$			$0.3 \times V_{CC}$	
Low- level output current	$I_{OL}$	$V_{CC} = 1.65V$			4	mA
		$V_{CC} = 2.3V$			8	
		$V_{CC} = 3V$			16	
		$V_{CC} = 3V$			24	
		$V_{CC} = 4.5V$			32	
Input transition rise or fall rate	$\Delta T/\Delta V$	$V_{CC} = 1.8V \pm 0.15V, 2.5V \pm 0.2V$			20	ns/V
		$V_{CC} = 3.3V \pm 0.3V$			10	
		$V_{CC} = 5V \pm 0.5V$			5	
Operating temperature	$T_A$		-40		125	$^{\circ}C$

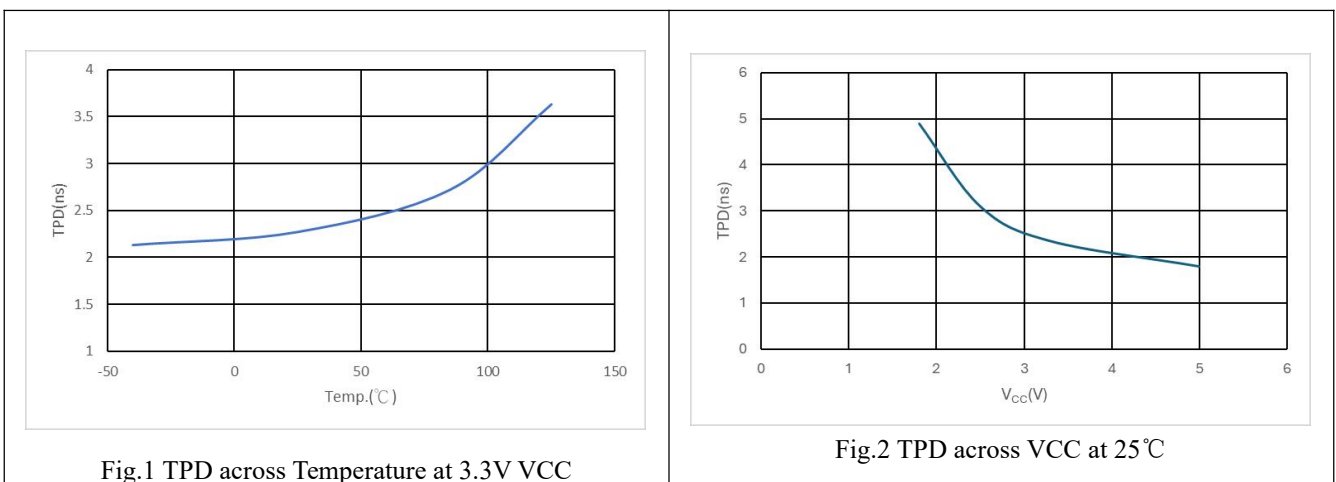
## Electrical Characteristics

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Low- level output voltage	$V_{OL}$	$V_{CC} = 1.65 \sim 5.5V, I_{OL} = 100\mu A$			0.1	V
		$V_{CC} = 1.65V, I_{OL} = 4mA$			0.45	
		$V_{CC} = 2.3V, I_{OL} = 8mA$			0.3	
		$V_{CC} = 3V, I_{OL} = 16mA$			0.4	
		$V_{CC} = 3V, I_{OL} = 24mA$			0.55	
		$V_{CC} = 4.5V, I_{OL} = 32mA$			0.55	
Input leakage current	$I_I$	$V_{IN} = 5.5V$ or GND, $V_{CC} = 0 \sim 5.5V$			$\pm 5$	$\mu A$
Power off leakage current	$I_{OFF}$	$V_I$ or $V_O = 5.5V, V_{CC} = 0V$			$\pm 10$	$\mu A$
Supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0, V_{CC} = 1.65 \sim 5.5V$			10	$\mu A$
Additional supply current per input pin	$\Delta I_{CC}$	$V_{CC} = 3 \sim 5.5V$ , one input at $V_{CC} - 0.6V$ , other input at $V_{CC}$ or GND			500	$\mu A$

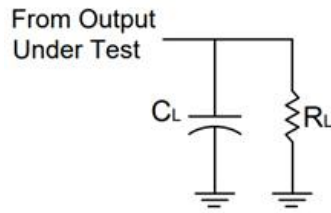
## Switching Characteristics

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit		
Propagation delay from input(A or B) to output(Y)	$T_{PD}$	$V_{CC} = 1.8V \pm 0.15V$	$C_L = 15pF$ $R_L = 1M\Omega$			1.5	ns	
		$V_{CC} = 2.5V \pm 0.2V$				0.7		4.4
		$V_{CC} = 3.3V \pm 0.3V$				0.8		3.6
		$V_{CC} = 5V \pm 0.5V$				0.8		3.4

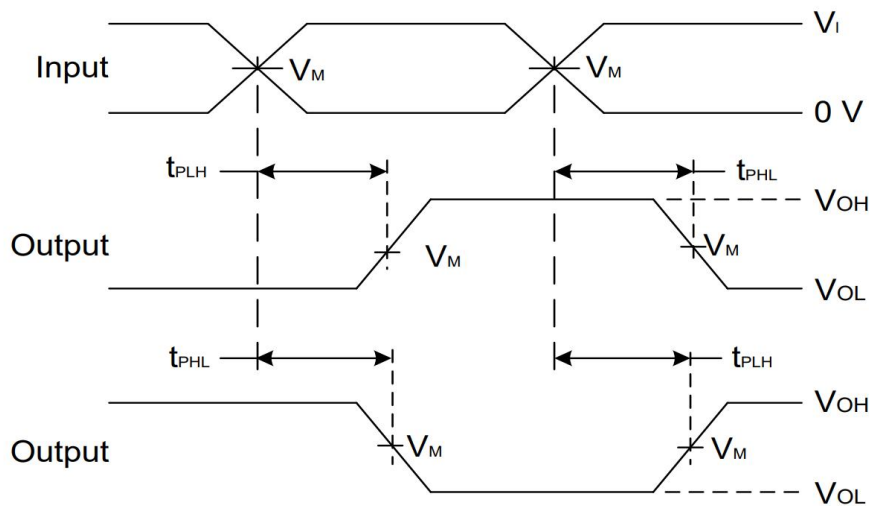
## Typical Characteristics



## Parameter Measurement Information



V <sub>CC</sub>	INPUTS		V <sub>M</sub>	C <sub>L</sub>	R <sub>L</sub>
	V <sub>I</sub>	t <sub>r</sub> /t <sub>f</sub>			
1.8V ± 0.15V	V <sub>CC</sub>	≅ 2ns	V <sub>CC</sub> /2	15pF	1MΩ
2.5V ± 0.2V	V <sub>CC</sub>	≅ 2ns	V <sub>CC</sub> /2	15pF	1MΩ
3.3V ± 0.3V	3V	≅ 2.5ns	1.5V	15pF	1MΩ
5V ± 0.5V	V <sub>CC</sub>	≅ 2.5ns	V <sub>CC</sub> /2	15pF	1MΩ



Voltage Waveform Propagation Delay Times  
Inverting and Non Inverting Outputs

- Notes:
- A. C<sub>L</sub> includes probe and jig capacitance
  - B. All pulses and supplied at pulse repetition rate ≅ 10MHz
  - C. The Inputs are measured separately one transition per measurement
  - D. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>PD</sub>

## IC Operation Information

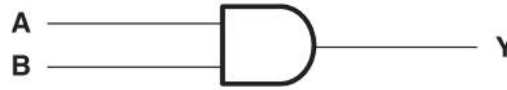
### Basic Operation

The FLG74LVC1G08 device contains one 2-input positive AND gate device and performs the Boolean function  $Y = A \cdot B$

B or  $Y = \overline{A + B}$ . This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry

disables the outputs, preventing damaging current backflow through the device when it is powered down.

## Function Block Diagram



## Feature Description

- Wide operating voltage range.  
-Operates from 1.65 V to 5.5 V.
- Allows down voltage translation.
- Inputs accept voltages to 5.5 V.
- Ioff feature allows voltages on the inputs and outputs when  $V_{CC}$  is 0 V.

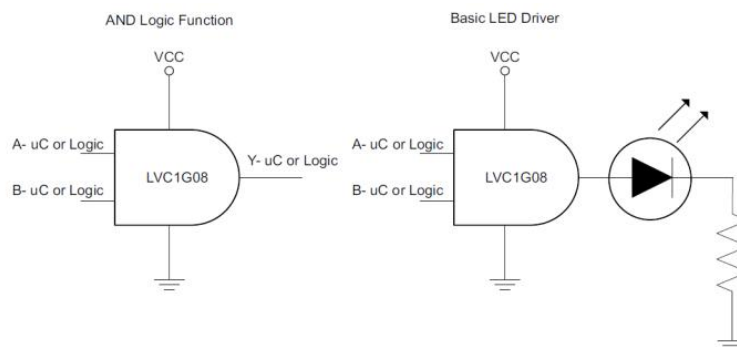
## Device Functional Table

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

## IC Application Information

The FLG74LVC1G08 is a high drive CMOS device that can be used for implementing AND logic with a high output drive, such as an LED application. It can produce 24 mA of drive current at 3.3 V making it Ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5 V tolerant allowing it to translate down to  $V_{CC}$ .

## Typical Application



## Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

## Detailed Design Procedure

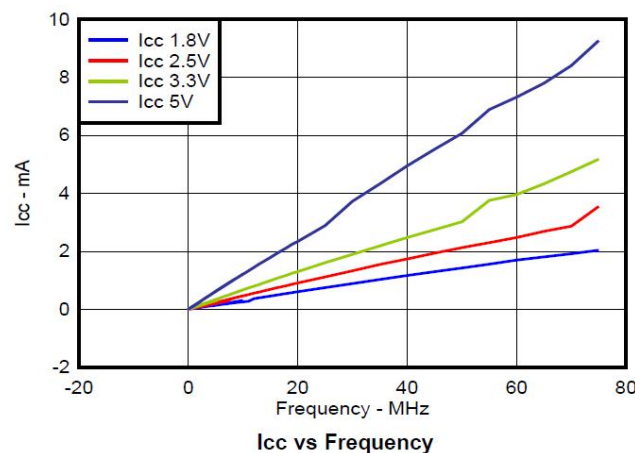
### 1. Recommended Input Conditions

- Rise time and fall time specs. See ( $\Delta t / \Delta V$ ) in the Recommended Operating Conditions table.
- Specified high and low levels. See ( $V_{IH}$  and  $V_{IL}$ ) in the Recommended Operating Conditions table
- Inputs are overvoltage tolerant allowing them to go as high as ( $V_I \max$ ) in the Recommended Operating Conditions table at any valid  $V_{CC}$ .

### 2. Recommend Output Conditions

- Load currents should not exceed ( $I_O \max$ ) per output and should not exceed total current (continuous current through  $V_{CC}$  or GND) for the part. These limits are located in the Absolute Maximum Ratings table.
- Outputs should not be pulled above  $V_{CC}$ .

## Application Curves



## Power Supply Recommendations

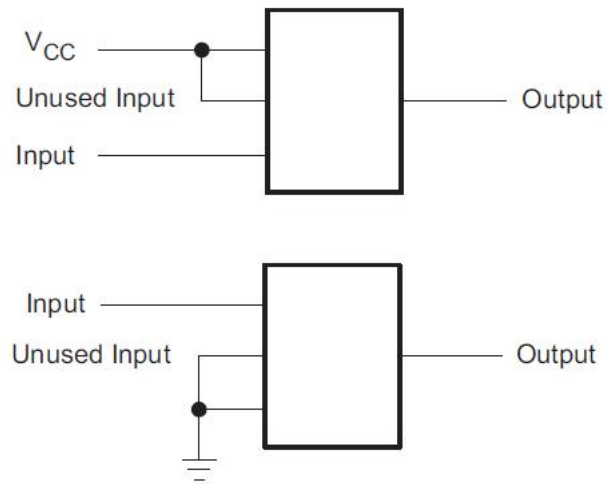
The power supply can be any voltage between the min and max supply voltage rating located in the Recommended Operating Conditions table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- $\mu F$  capacitor is recommended and if there are multiple  $V_{CC}$  pins then 0.01- $\mu F$  or 0.022- $\mu F$  capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- $\mu F$  and 1- $\mu F$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## Layout Considerations

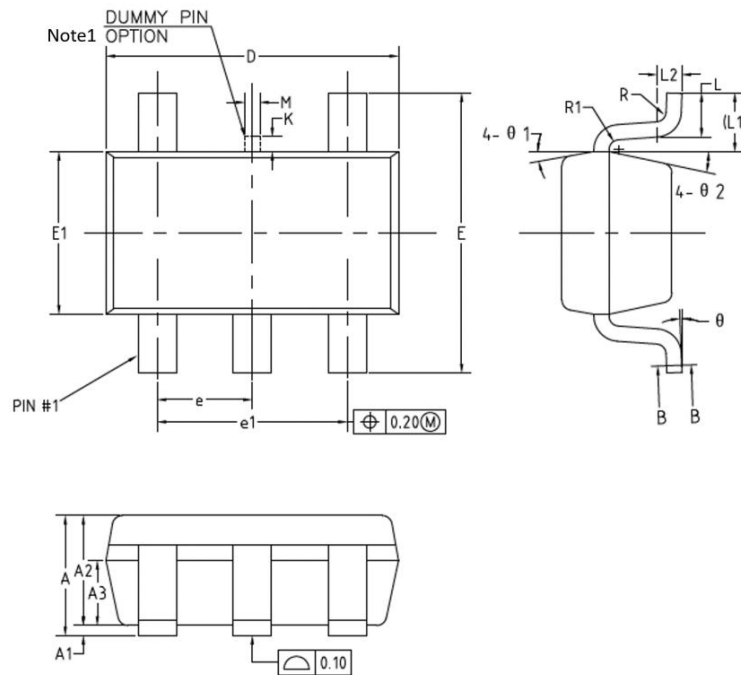
When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input buffer gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside

connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or VCC whichever make more sense or is more convenient.



## Package Information

(1) Package Type: SOT23-5

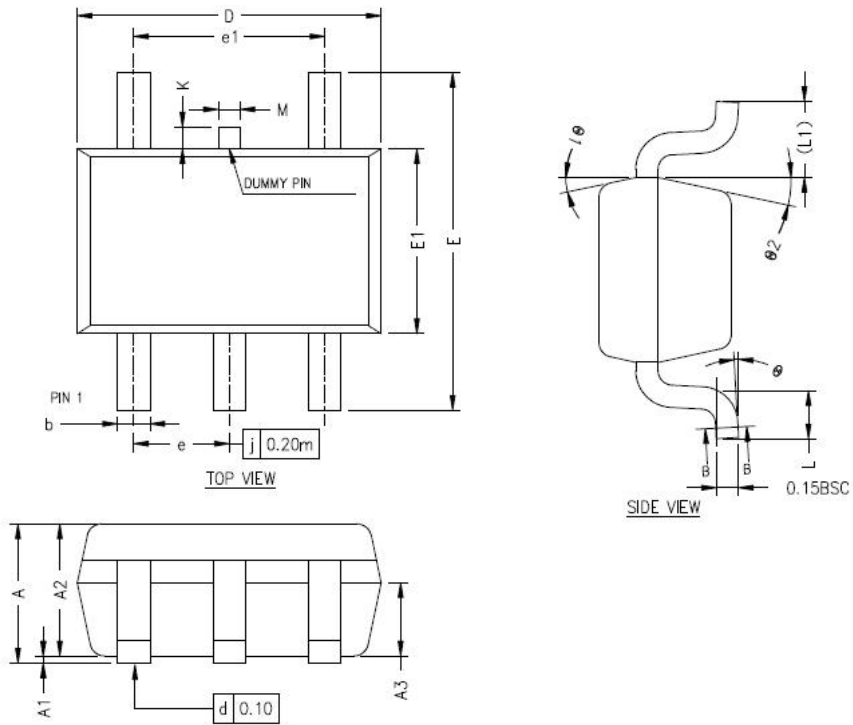


COMMON DIMENSIONS  
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.25
A1	0	—	0.15
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
⚠ b	0.34	—	0.45
⚠ b1	0.34	0.38	0.41
⚠ c	0.12	—	0.20
⚠ c1	0.12	0.15	0.16
D	2.826	2.926	3.026
E	2.60	2.80	3.00
⚠ E1	1.526	1.626	1.700
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
⚠ K	0	—	0.20
L	0.30	0.40	0.60
L1	0.59REF		
L2	0.25BSC		
⚠ M	0.10	0.15	0.20
R	0.05	—	0.20
R1	0.05	—	0.20
θ	0°	—	8°
θ 1	8°	10°	12°
θ 2	10°	12°	14°

Notes: 1. Dummy pin may differ or may not be present.

(2) Package Type: SC70



COMMON DIMENSIONS  
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.80	—	1.10
A1	0	—	0.10
A2	0.80	0.90	1.00
A3	0.40	0.50	0.60
b	0.17	—	0.30
b1	0.17	0.22	0.25
c	0.12	—	0.20
c1	0.12	0.15	0.16
D	2.02	2.07	2.12
E	2.20	2.30	2.40
E1	1.21	1.26	1.31
e	0.60	0.65	0.70
e1	1.20	1.30	1.40
L	0.26	0.33	0.46
L1	0.52REF		
M	0.10	0.15	0.20
K	0	—	0.20
θ	0°	—	8°
θ1	10°	12°	14°
θ2	10°	12°	14°

## Important Notice And Disclaimer

- We reserves the right to change the instruction manual without prior notice.
- Any semiconductor product has a certain possibility of failure or malfunction under specific conditions. The buyer is responsible for complying with safety standards and taking safety measures when using our products for system design and overall manufacturing to avoid potential failure risks that may cause personal injury or property damage.
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