2-Input Positive-AND Gate

Description

This single 2-input AND buffer gate with open-drain output is designed for 1.65-V to 5.5-V VCC operation.

The FLG74LVC1G09 device performs the Boolean function Y=AxB in positive logic.

The CMOS device has high output drive while maintaining low static power dissipation over a broad VCC operating range.

The FLG74LVC1G09 is available in a variety of packages, including the ultra-small DFN package with a body size of 1 mm ×1 mm.

Features

- Inputs Accept Voltages 1.65V to 5.5 V
- Max Tpd of 3.6 ns at 3.3 V
- Low Power Consumption, 10- μA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

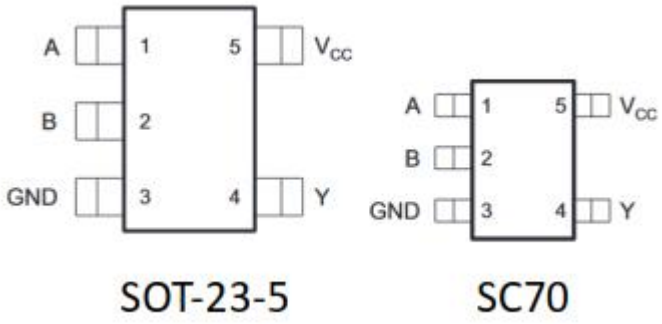
Applications

- AV Receiver
- Audio Dock: Portable
- Blu-ray Player and Home Theater
- Embedded PC
- MP3 Player/Recorder (Portable Audio)
- Personal Digital Assistant (PDA)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid State Drive (SSD): Client and Enterprise
- TV: LCD/Digital and High-Definition (HDTV)
- Tablet: Enterprise
- Video Analytics: Server
- Wireless Headset, Keyboard, and Mouse

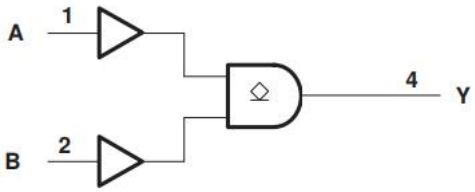
Order information

Mode	Package	Ordering Number	Packing Option
FLG74LVC1G09	SOT23-5	FLG74LVC1G09YSOT235G/TR	Tape and Reel,3000
	SC70	FLG74LVC1G09YSC70G/TR	Tape and Reel,3000

Pin Configuration



Simplified Schematic



Pin Assignment

Pin Name	Pin No.	Pin Function
A	1	Input
B	2	Input
GND	3	Ground
Y	4	Output
VCC	5	Power Pin

Absolute Maximum Ratings (Note1)

- V_{CC} ---------- -0. 5V to + 6.5V
- V_I ---------- - 0. 5V t o + 6.5V
- V_O (Voltage range applied to any output in the high-impedance or power-off state) ---------- - 0. 5V to + 6.5V
- V_O(Voltage range applied to any output in the high or slow state)---------- -0.5V to V_{CC}+0.5V
- Input clamp current ---------- -50mA
- Output clamp current ---------- -50mA
- Continuous output current ---------- ±50mA
- Storage Temperature ---------- -65℃ to 150℃

Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply voltage	V_{CC}	Operating	1.65		5.5	V
		Data retention only	1.5			
Input voltage	V_I		0		5.5	V
Output voltage	V_O				VCC	V
High- level input voltage	V_{IH}	V_{CC} = 1.65V to 1.95V	0.65×V_{CC}			V
		V_{CC} = 2.3V to 2.7V	1.7			
		V_{CC} = 3V to 3.6V	2			
		V_{CC} = 4.5V to 5.5V	0.7×V_{CC}			
Low- level input voltage	V_{IL}	V_{CC} = 1.65V to 1.95V			0.35×V_{CC}	V
		V_{CC} = 2.3V to 2.7V			0.7	
		V_{CC} = 3V to 3.6V			0.8	
		V_{CC} = 4.5V to 5.5V			0.3×V_{CC}	
Low- level output current	I_{OL}	V_{CC} = 1.65V			4	mA
		V_{CC} = 2.3V			8	
		V_{CC} = 3V			16	
		V_{CC} = 3V			24	
		V_{CC} = 4.5V			32	
Input transition rise or fall rate	△T/△V	V_{CC} = 1.8V±0.15V, 2.5V±0.2V			20	ns/V
		V_{CC} =3.3V±0.3V			10	
		V_{CC} =5V±0.5V			5	
Operating temperature	T_A		-40		125	℃

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Low- level output voltage	V_{OL}	V_{CC} =1.65~5.5V, I_{OL}= 100uA			0.1	V
		VCC = 1.65V, IOL= 4mA			0.45	
		VCC = 2.3V, IOL= 8mA			0.3	
		VCC = 3V, IOL= 16mA			0.4	
		VCC = 3V, IOL= 24mA			0.55	
		VCC = 4.5V, IOL= 32mA			0.55	
Input leakage current	I_I	V_{IN}= 5.5V or GND, V_{CC}= 0~5.5V			±5	uA
Power off leakage current	I_{OFF}	V_I or V_O=5.5V, V_{CC}=0V			±10	uA
Supply current	I_{CC}	V_{IN}= VCC or GND , I_{OUT}=0,V_{CC}= 1.65~5.5V			10	uA
Additional supply current per input pin	$\triangle I_{CC}$	V_{CC}=3~5.5V, one input ate V_{CC}-0.6V, other input at V_{CC} or GND			500	uA

Switching Characteristics

Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Propagation delay from input(A or B) to output(Y)	T_{PD}	V_{CC} =1.8V±0.15V,R_L=1KΩ	C_L=30pF	1		13.6	ns
		V_{CC} = 2.5V±0.2V,R_L=500Ω		0.5		9.8	
		V_{CC} = 3.3V±0.3V,R_L=500Ω	C_L=50pF	1		7.5	
		V_{CC} = 5V±0.5V,R_L=500Ω		0.5		6.6	

Typical Characteristics

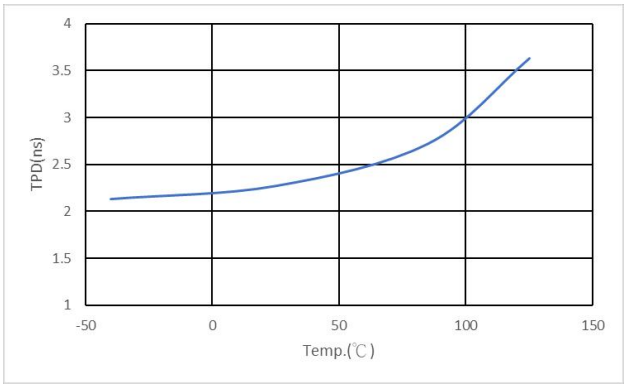


Fig.1 TPD across Temperature at 3.3V VCC

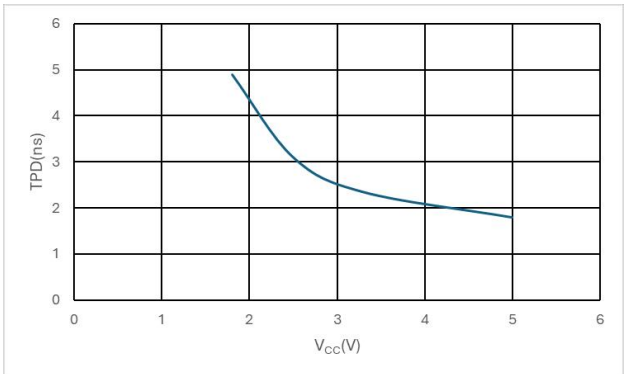
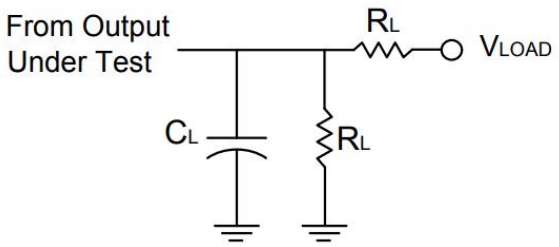


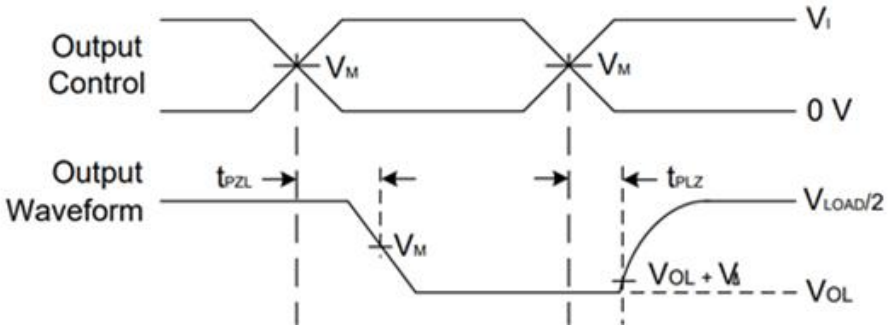
Fig.2 TPD across VCC at 25℃

Parameter Measurement Information



TEST	Condition
t_{PLZ}	V_{LOAD}
t_{PZL}	V_{LOAD}

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V△
	V_I	t_r/t_f					
1.8V ± 0.15V	V_{CC}	≦2ns	$V_{CC}/2$	$2\times V_{CC}$	30pF	1kΩ	0.15V
2.5V ± 0.2V	V_{CC}	≦2ns	$V_{CC}/2$	$2\times V_{CC}$	30pF	500Ω	0.15V
3.3V ± 0.3V	3V	≦2.5ns	1.5V	6V	50pF	500Ω	0.3V
5V ± 0.5V	V_{CC}	≦2.5ns	$V_{CC}/2$	$2\times V_{CC}$	50pF	500Ω	0.3V



Voltage Waveform Enable and DisableTimes

Low- and High-Level Enabling

Notes: A. C_L includes probe and jig capacitance

B. All pulses and supplied at pulse repetition rate ≦ 10MHz

C. The Inputs are measured one at a time with one transition per measurement

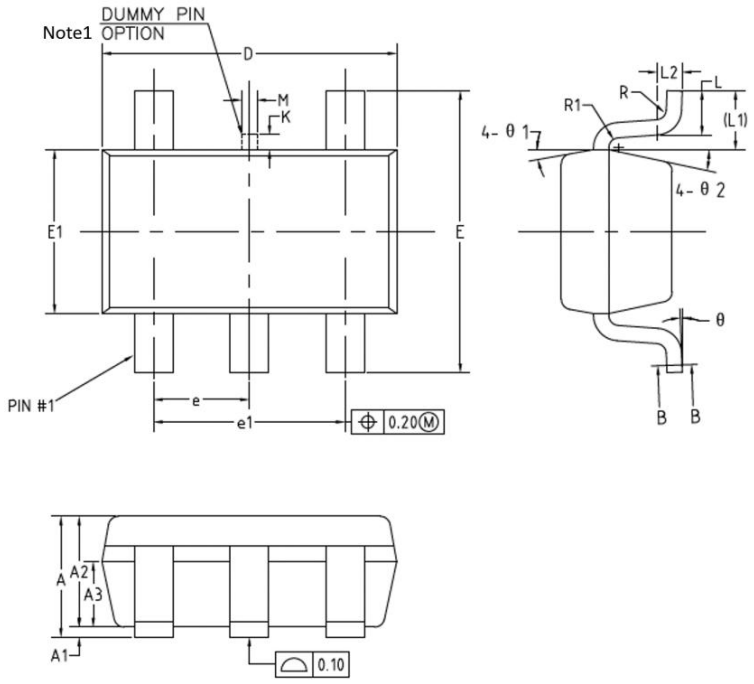
D. For the open drain device t_{PLZ} and t_{PZL} are the same as t_{PD}

E. t_{PZL} is measured at V_M

F. t_{PLZ} is measured at V_{OL} + V△

Package Information

(1) Package Type: SOT23-5

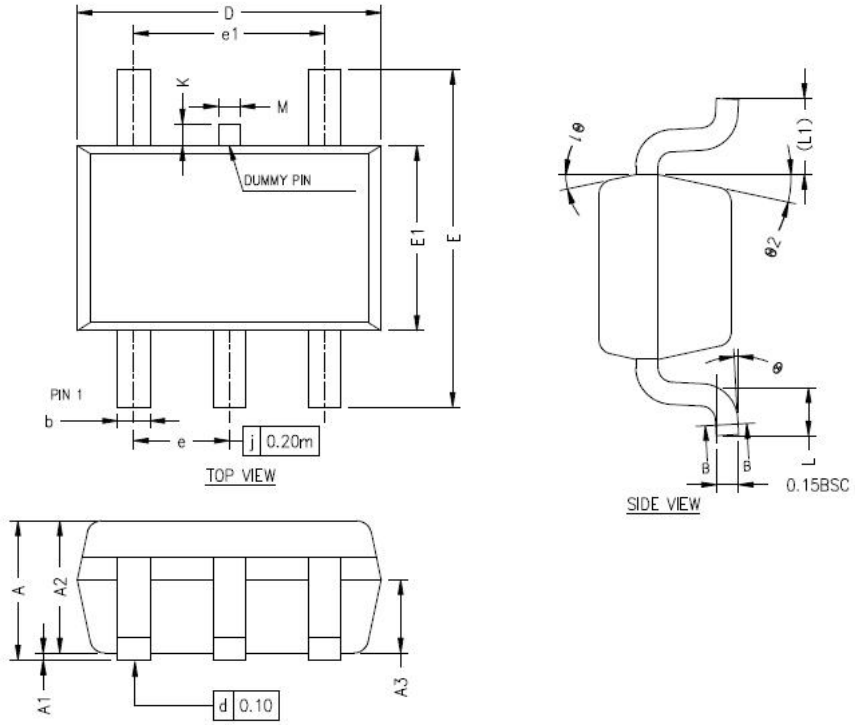


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

	SYMBOL	MIN	NOM	MAX
	A	–	–	1.25
	A1	0	–	0.15
	A2	1.00	1.10	1.20
	A3	0.60	0.65	0.70
4	b	0.34	–	0.45
4	b1	0.34	0.38	0.41
4	c	0.12	–	0.20
4	c1	0.12	0.15	0.16
	D	2.826	2.926	3.026
	E	2.60	2.80	3.00
3	E1	1.526	1.626	1.700
	e	0.90	0.95	1.00
	e1	1.80	1.90	2.00
2	K	0	–	0.20
	L	0.30	0.40	0.60
	L1		0.59REF	
	L2		0.25BSC	
2	M	0.10	0.15	0.20
	R	0.05	–	0.20
	R1	0.05	–	0.20
	θ	0°	–	8°
	θ 1	8°	10°	12°
	θ 2	10°	12°	14°

Notes: 1. Dummy pin may differ or may not be present.

(2) Package Type: SC70



COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

	SYMBOL	MIN	NOM	MAX
	A	0.80	–	1.10
	A1	0	–	0.10
	A2	0.80	0.90	1.00
	A3	0.40	0.50	0.60
	b	0.17	–	0.30
	b1	0.17	0.22	0.25
3	c	0.12	–	0.20
3	c1	0.12	0.15	0.16
	D	2.02	2.07	2.12
	E	2.20	2.30	2.40
	E1	1.21	1.26	1.31
	e	0.60	0.65	0.70
	e1	1.20	1.30	1.40
	L	0.26	0.33	0.46
	L1	0.52REF		
2	M	0.10	0.15	0.20
2	K	0	–	0.20
	θ	0°	–	8°
	θ1	10°	12°	14°
	θ2	10°	12°	14°

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