FLG74LVC2G04 Single Inverter Gate

Description

This dual inverter is designed for 1.65-V to 5.5-V VCC operation.

The FLG74LVC2G04 device performs the Boolean function $Y = \overline{A}$.

This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The FLG74LVC2G04 device is available in a variety of packages, including SOT-23, SOT-353, SOT553.

Features

- Supports 5-V V_{CC} Operation
- Max Tpd of 4.1 ns at 3.3 V
- Low Power Consumption, 10- μA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- Typical V_{OLP} (Output Ground Bounce) <0.8V at V_{CC} = 3.3V, TA = 25℃
- Typical V_{OHV} (Output VOH Undershoot) > 2V at V_{CC} = 3.3V, TA = 25℃
- I_{off} Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

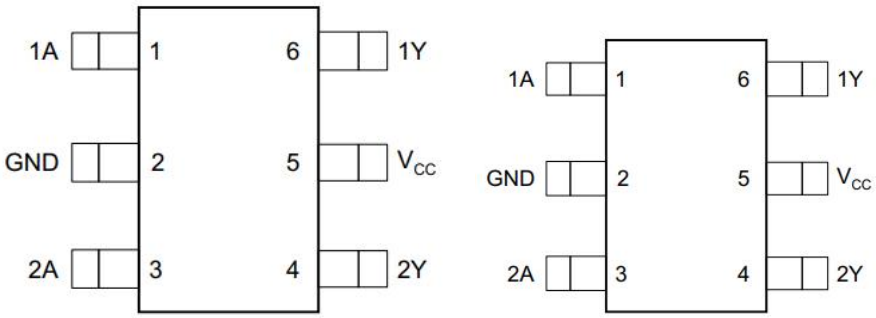
Applications

- IP Phones: Wired and Wireless
- Optical Modules
- Optical Networking: EPON and Video Over Fiber
- Point-to-Point Microwave Backhaul
- Power: Telecom DC/DC Module: Analog and Digital
- Private Branch Exchanges (PBX)
- TETRA Base Exchanges
- Telecom Base Band Units
- Tablet: Enterprise
- Telecom Shelters: Power Distribution Units (PDU), Power Monitoring Units (PMU), Wireless Battery Monitoring, Remote Electrical Tilt Units (RET), Remote Radio Units (RRU), Tower Mounted 1 Amplifiers (TMA)
- Vector Signal Analyzers and Generators

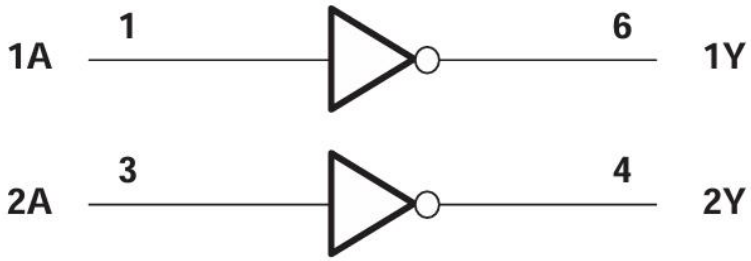
Order information

Mode	Package	Ordering Number	Packing Option
FLG74LVC2G04	SOT23-6	FLG74LVC2G04YSOT236G/TR	Tape and Reel,3000
	SC70-6	FLG74LVC2G04YSC706G/TR	Tape and Reel,3000

Pin Configuration



Simplified Schematic



Pin Assignment

Pin Name	Pin No.	Pin Function
GND	2	Ground
1A	1	Input 1
2A	3	Input 2
1Y	6	Open-drain output 1
2Y	4	Open-drain output 2
VCC	5	Power pin

Absolute Maximum Ratings (Note1)

- V_{CC} ---------- -0. 5V to + 6.5V
- V_I ---------- - 0. 5V t o + 6.5V
- V_O (Voltage range applied to any output in the high-impedance or power-off state) ---------- - 0. 5V to + 6.5V
- V_O(Voltage range applied to any output in the high or slow state)---------- -0.5V to V_{CC}+0.5V
- Input clamp current ---------- -50mA
- Output clamp current ---------- -50mA
- Continuous output current ---------- ±50mA
- Storage Temperature ---------- -65℃ to 150℃

Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply voltage	V_{CC}	Operating	1.65		5.5	V
		Data retention only	1.5			
Input voltage	V_I		0		5.5	V
Output voltage	V_O				VCC	V
High- level input voltage	V_{IH}	V_{CC} = 1.65V to 1.95V	0.65×V_{CC}			V
		V_{CC} = 2.3V to 2.7V	1.7			
		V_{CC} = 3V to 3.6V	2			
		V_{CC} = 4.5V to 5.5V	0.7×V_{CC}			
Low- level input voltage	V_{IL}	V_{CC} = 1.65V to 1.95V			0.35×V_{CC}	V
		V_{CC} = 2.3V to 2.7V			0.7	
		V_{CC} = 3V to 3.6V			0.8	
		V_{CC} = 4.5V to 5.5V			0.3×V_{CC}	
High- level output current	I_{OH}	V_{CC} = 1.65V			-4	mA
		V_{CC} = 2.3V			-8	
		V_{CC} = 3V			-16	
		V_{CC} = 3V			-24	
		V_{CC} = 4.5V			-32	
Low- level output current	I_{OL}	V_{CC} = 1.65V			4	mA
		V_{CC} = 2.3V			8	
		V_{CC} = 3V			16	
		V_{CC} = 3V			24	
		V_{CC} = 4.5V			32	
Input transition rise or fall rate	△T/△V	V_{CC} = 1.8V±0.15V, 2.5V±0.2V			20	ns/V
		V_{CC} =3.3V±0.3V			10	
		V_{CC} =5V±0.5V			5	
Operating temperature	T_A		-40		125	℃

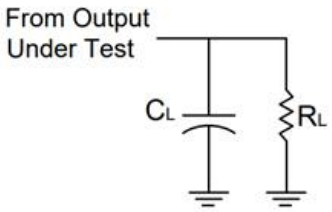
Electrical Characteristics

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
High- level output voltage	V_{OH}	V_{CC} = 1.65~5.5V, I_{OH}= -100uA	V_{CC}-0.1			V
		V_{CC} = 1.65V, I_{OH}= -4mA	1.2			
		V_{CC} = 2.3V, I_{OH}= -8mA	1.9			
		V_{CC} = 3V, I_{OH}= -16mA	2.4			
		V_{CC} = 3V, I_{OH}= -24mA	2.3			
		V_{CC} = 4.5V, I_{OH}= -32mA	3.8			
Low- level output voltage	V_{OL}	V_{CC} =1.65~5.5V, I_{OL}= 100uA			0.1	V
		VCC = 1.65V, IOL= 4mA			0.45	
		VCC = 2.3V, IOL= 8mA			0.3	
		VCC = 3V, IOL= 16mA			0.4	
		VCC = 3V, IOL= 24mA			0.55	
		VCC = 4.5V, IOL= 32mA			0.55	
Input leakage current	I_I	V_{IN}= 5.5V or GND, V_{CC}= 0~5.5V			±5	uA
Power off leakage current	I_{OFF}	V_I or V_O=5.5V, V_{CC}=0V			±10	uA
Supply current	I_{CC}	V_{IN}= VCC or GND , I_{OUT}=0,V_{CC}= 1.65~5.5V			10	uA
Additional supply current per input pin	$\triangle I_{CC}$	V_{CC}=3~5.5V, one input ate V_{CC}-0.6V, other input at V_{CC} or GND			500	uA

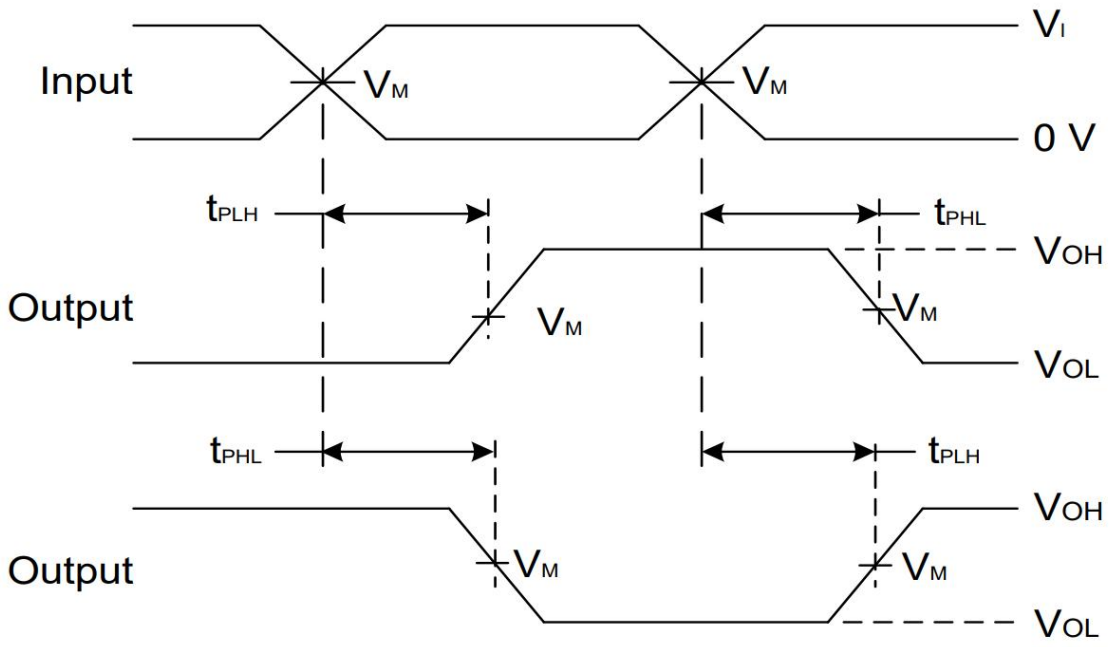
Switching Characteristics

Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Propagation delay from input(A) to output(Y)	T_{PD}	V_{CC} = 1.8V±0.15V	C_L=15pF R_L=1MΩ	3.1		8	ns
		V_{CC} = 2.5V±0.2V		1.5		4.4	
		V_{CC} = 3.3V±0.3V		1.2		4.1	
		V_{CC} = 5V±0.5V		1		3.2	

Parameter Measurement Information



V_{CC}	INPUTS		V_M	C_L	R_L
	V_I	t_r/t_f			
1.8V ± 0.15V	V_{CC}	≦2ns	$V_{CC}/2$	15pF	1MΩ
2.5V ± 0.2V	V_{CC}	≦2ns	$V_{CC}/2$	15pF	1MΩ
3.3V ± 0.3V	3V	≦2.5ns	1.5V	15pF	1MΩ
5V ± 0.5V	V_{CC}	≦2.5ns	$V_{CC}/2$	15pF	1MΩ



Voltage Waveform Propagation Delay Times

Inverting and Non Inverting Outputs

Notes: A. C_L includes probe and jig capacitance

B. All pulses and supplied at pulse repetition rate ≦ 10MHz

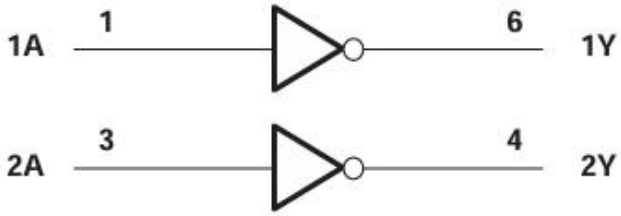
C. t_{PLH} and t_{PHL} are the same as t_{PD}

IC Operation Information

Basic Operation

The FLG74LVC2G04 contains two identical inverters that operate from 1.65-V to 5.5-V VCC. Each inverter has a balanced output capable of outputting 32 mA at V_{CC}=4.5 ~V.\) The overvoltage tolerant inputs allow for down translation of up to 6.5 V, and the partial power-off feature ensures that the inputs and outputs can be any value from –0.5 V to 6.5 V when VCC is 0 V

Function Block Diagram



Feature Description

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package. This device supports 5-V VCC operation and up to 5.5-V inputs. It has a low propagation delay of only 4.1 ns at 3.3 V.Power consumption is low with only 10- μ A Max ICC. Balanced drive output at 3.3 V can put out ±24-mA. Typical output ground bounce is less than 0.8 V at 3.3-V VCC and typical output undershoot is greater than 2 V at 3.3-V VCC.
This device supports partial-power-down mode operation.

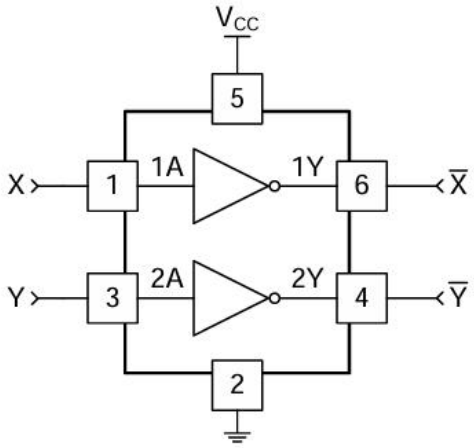
Device Functional Table

INPUT A	OUTPUT Y
H	Hi-Z
L	L

IC Application Information

The FLG74LVC2G04 contains two logic inverters. It can be used in a wide variety of applications, with this being one example. Because this part has overvoltage tolerant inputs, it can be used for down translating logic levels. This example explains the method used for down-translating with this logic gate.

Typical Application



Design Requirements

this device can be any value from–0.5 V to 6.5 V, according to Absolute Maximum Ratings. Because the input limits are not associated with V_{CC} down-translation is simple. The output voltage is selected with V_{CC} , and so long as the input logic voltage is larger than V_{IH} , found in Recommended Operating Conditions, the output will trigger properly.

Detailed Design Procedure

1. Recommended Input Conditions
   - – Rise time and fall time specs. See (Δ t/ Δ V) in the Recommended Operating Conditions table.
   - – Specified high and low levels. See(V_{IH} and V_{IL}) in the Recommended Operating Conditions table
   - – Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the Recommended Operating Conditions table at any valid V_{CC}.
2. Recommend Output Conditions
   - – Load currents should not exceed (I_O max) per output and should not exceed total current (continuous current through (V_{CC} or GND) for the part. These limits are located in the Absolute Maximum Ratings table.
   - – Outputs should not be pulled above V_{CC}.

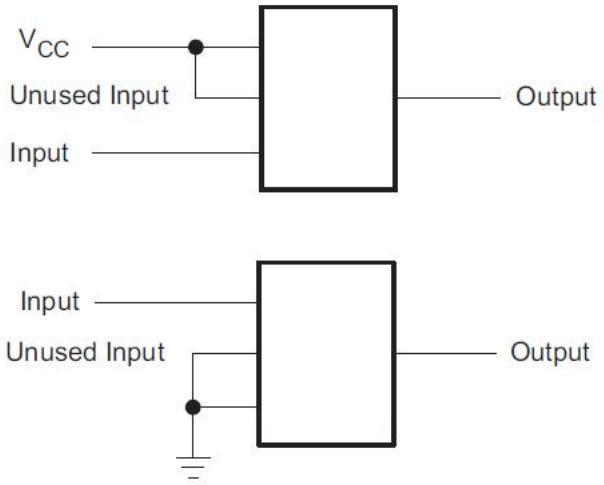
Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the Recommended Operating Conditions table.

Each Vcc pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF capacitor is recommended and if there are multiple Vcc pins then 0.01-µF or 0.022-µF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

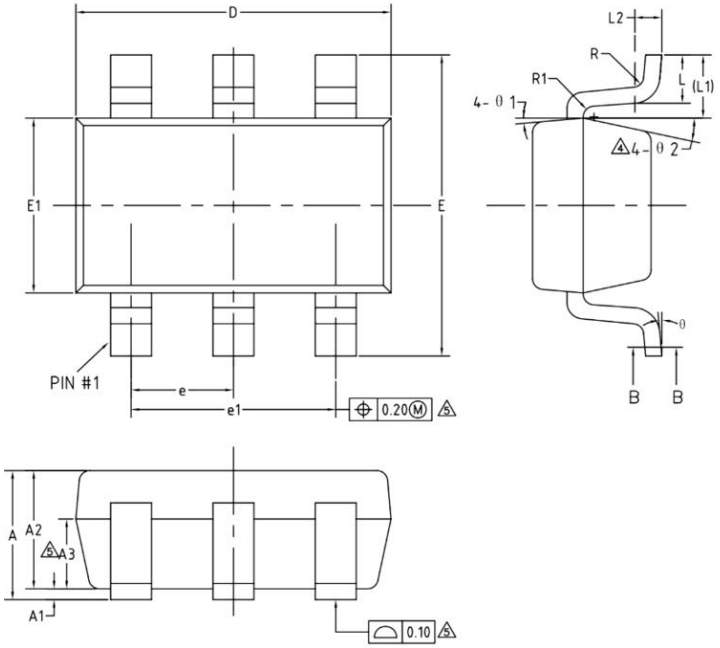
Layout Considerations

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or VCC whichever make more sense or is more convenient.



Package Information

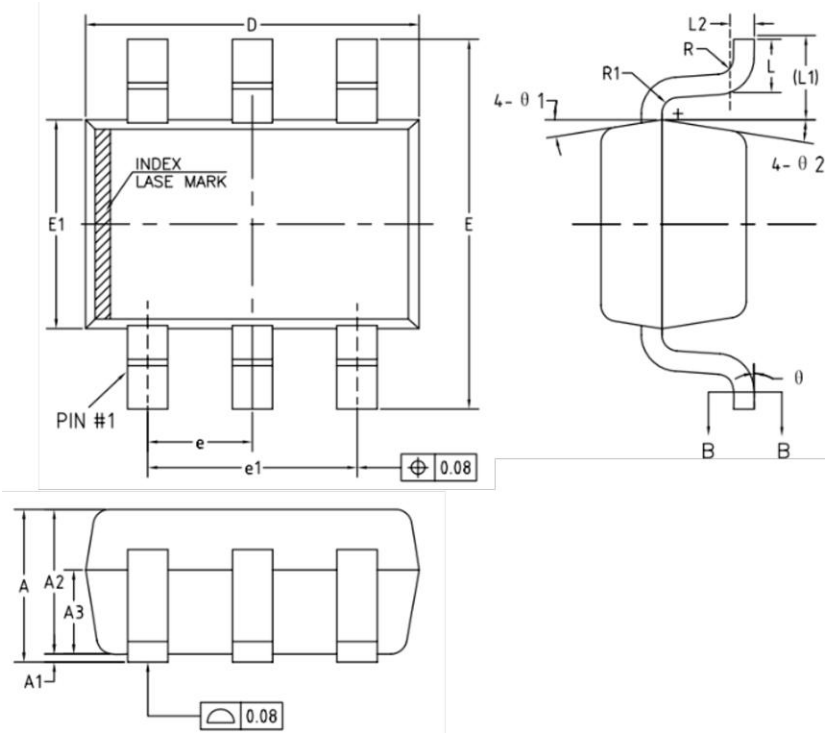
(1) Package Type: SOT23-6



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

	SYMBOL	MIN	NOM	MAX
	A	–	–	1.25
	A1	0	–	0.15
	A2	1.00	1.10	1.20
	A3	0.60	0.65	0.70
	b	0.36	–	0.50
	b1	0.36	0.38	0.45
	c	0.14	–	0.20
	c1	0.14	0.15	0.16
	D	2.826	2.926	3.026
	E	2.60	2.80	3.00
	E1	1.526	1.626	1.726
4	e	0.90	0.95	1.00
4	e1	1.80	1.90	2.00
	L	0.35	0.45	0.60
	L1	0.59REF		
	L2	0.25BSC		
3	R	0.10	–	–
3	R1	0.10	–	0.20
	θ	0°	–	8°
	θ 1	3°	5°	7°
4	θ 2	6°	–	14°

(2) Package Type: SC70



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.85	–	1.05
A1	0	–	0.10
A2	0.80	0.90	1.00
A3	0.47	0.52	0.57
2 b	0.22	–	0.29
b1	0.22	0.25	0.28
3 2 c	0.115	–	0.15
3 c1	0.115	0.13	0.14
D	2.02	2.07	2.12
E	2.20	2.30	2.40
E1	1.25	1.30	1.35
e	0.65BSC		
e1	1.30BSC		
L	0.28	0.33	0.38
L1	0.50REF		
L2	0.15BSC		
R	0.10	–	–
R1	0.10	–	0.25
θ	0°	–	8°
θ 1	6°	9°	12°
θ 2	6°	9°	12°

Important Notice And Disclaimer

- We reserves the right to change the instruction manual without prior notice.
- Any semiconductor product has a certain possibility of failure or malfunction under specific conditions. The buyer is responsible for complying with safety standards and taking safety measures when using our products for system design and overall manufacturing to avoid potential failure risks that may cause personal injury or property damage.
- The improvement of product quality is endless, our company will be dedicated to provide customers with better products.