Dual Schmitt-Trigger Inverter

Description

This dual Schmitt-trigger inverter is designed for 1.65-V to5.5-V V_{CC} operation.

The FLG74LVC2G14 device contains two inverters and performs the Boolean function $Y = \overline{A}$ The device functions as two independent inverters, but because of Schmitt action, it may have different input threshold levels for positive-going V_{T+} and negative-going V_{T-} signals.

This device is fully specified for partial-power-down applications using Ioff. The I loff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Features

- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max Tpd of 5.4 ns at 3.3 V
- Low Power Consumption, 10-μA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8V at V_{CC} = 3.3V, TA = 25℃
- Typical V_{OHV} (Output VOH Undershoot) > 2V at V_{CC} = 3.3V, TA = 25℃
- I_{OFF} Supports Live Insertion, Partial-Power-Down-Mode and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

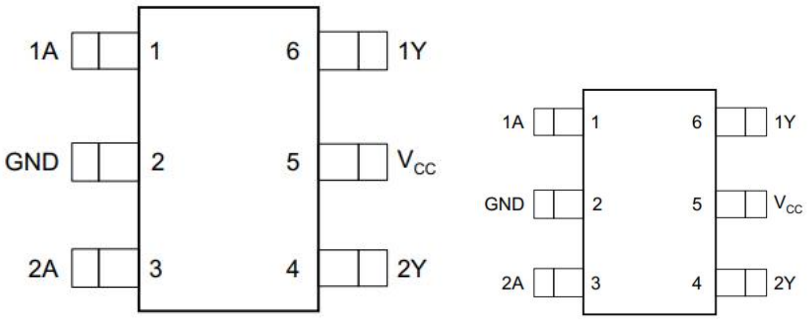
Applications

- Body Control Modules
- Engine Control Modules
- Arcade, Casino, and Gambling Machines
- Servers and High-Performance Com-puting
- EPOS, ECR, and Cash Drawer
- Desktop PC

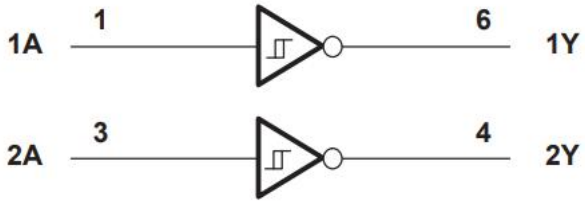
Order information

Mode	Package	Ordering Number	Packing Option
FLG74LVC2G14	SOT23-6	FLG74LVC2G14YSOT236G/TR	Tape and Reel,3000
	SC70-6	FLG74LVC2G14YSC706G/TR	Tape and Reel,3000

Pin Configuration



Simplified Schematic



Pin Assignment

Pin Name	Pin No.	Pin Function
GND	2	Ground
1A	1	Input 1
2A	3	Input 2
1Y	6	Open-drain output 1
2Y	4	Open-drain output 2
VCC	5	Power pin

Absolute Maximum Ratings (Note1)

- V_{CC} ---------- -0. 5V to + 6.5V
- V_I ---------- - 0. 5V t o + 6.5V
- V_O (Voltage range applied to any output in the high-impedance or power-off state) ---------- - 0. 5V to + 6.5V
- V_O(Voltage range applied to any output in the high or slow state)---------- -0.5V to V_{CC}+0.5V
- Input clamp current ---------- -50mA
- Output clamp current ---------- -50mA
- Continuous output current ---------- ±50mA
- Storage Temperature ---------- -65℃ to 150℃

Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply voltage	V_{CC}	Operating	1.65		5.5	V
Input voltage	V_I		0		5.5	V
Output voltage	V_O				VCC	V
High- level output current	I_{OH}	V_{CC} = 1.65V			-4	mA
		V_{CC} = 2.3V			-8	
		V_{CC} = 3V			-16	
		V_{CC} = 3V			-24	
		V_{CC} = 4.5V			-32	
Low- level output current	I_{OL}	V_{CC} = 1.65V			4	mA
		V_{CC} = 2.3V			8	
		V_{CC} = 3V			16	
		V_{CC} = 3V			24	
		V_{CC} = 4.5V			32	
Operating temperature	T_A		-40		125	℃

Electrical Characteristics

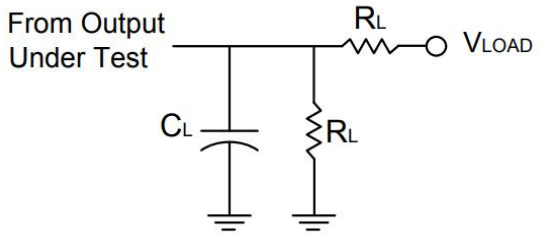
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Positive-going input threshold voltage	V_{T+}	V_{CC} = 1.65V	0.7		1.4	V
		V_{CC} = 2.3V	1		1.7	
		V_{CC} = 3V	1.3		2.2	
		V_{CC} = 4.5V	1.9		3.1	
		V_{CC} = 5.5V	2.2		3.7	
Negative-going input threshold voltage	V_{T-}	V_{CC} = 1.65V	0.3		0.7	V
		V_{CC} = 2.3V	0.4		1	
		V_{CC} = 3V	0.6		1.3	
		V_{CC} = 4.5V	1.1		2	

		V_{CC} = 5.5V	1.4		2.5	
Hysteresis voltage	△VT	V_{CC} = 1.65V	0.3		0.8	V
		V_{CC} = 2.3V	0.4		0.9	
		V_{CC} = 3V	0.4		1.1	
		V_{CC} = 4.5V	0.6		1.3	
		V_{CC} = 5.5V	0.7		1.4	
High- level output voltage	V_{OH}	V_{CC} = 1.65~5.5V, I_{OH}= 100uA	V_{CC}-0.1			V
		V_{CC} = 1.65V, I_{OH}= 4mA	1.2			
		V_{CC} = 2.3V, I_{OH}= 8mA	1.9			
		V_{CC} = 3V, I_{OH}= 16mA	2.4			
		V_{CC} = 3V, I_{OH}= 24mA	2.3			
		V_{CC} = 4.5V, I_{OH}= 32mA	3.8			
Low- level output voltage	V_{OL}	V_{CC} = 1.65~5.5V, I_{OL}= 100uA			0.1	V
		V_{CC} = 1.65V, I_{OL}= 4mA			0.45	
		V_{CC} = 2.3V, I_{OL}= 8mA			0.3	
		V_{CC} = 3V, I_{OL}= 16mA			0.4	
		V_{CC} = 3V, I_{OL}= 24mA			0.55	
		V_{CC} = 4.5V, I_{OL}= 32mA			0.55	
Input leakage current	I_I	V_{IN}= 5.5V or GND, V_{CC}= 0~5.5V			±5	uA
Power off leakage current	I_{OFF}	V_{IN} or V_O =5.5V, V_{CC}=0V			±10	uA
Supply current	I_{CC}	V_{IN}= VCC or GND , I_{OUT}=0,V_{CC}= 1.65~5.5V			10	uA
Additional supply current per input pin	△I_{CC}	V_{CC}=3~5.5V, one input ate V_{CC}-0.6V, other input at V_{CC} or GND			500	uA

Switching Characteristics

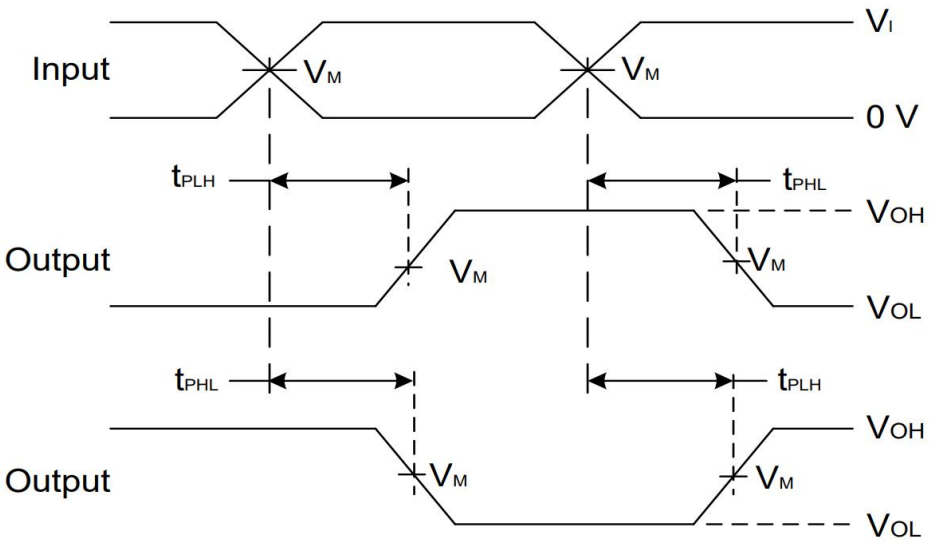
Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Propagation delay from input(A or B) to output(Y)	T_{PD}	V_{CC} =1.8V±0.15V,R_L=1KΩ	C_L=30pF	3.9		9.5	ns
		V_{CC} = 2.5V±0.2V,R_L=500Ω		1.9		5.7	
		V_{CC} = 3.3V±0.3V,R_L=500Ω	C_L=50pF	2		5.4	
		V_{CC} = 5V±0.5V,R_L=500Ω		1.5		4.3	

Parameter Measurement Information



TEST	Condition
t_{PLZ}	V_{LOAD}
t_{PZL}	V_{LOAD}

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V△
	V_I	t_r/t_f					
1.8V ± 0.15V	V_{CC}	≦2ns	$V_{CC}/2$	$2\times V_{CC}$	30pF	1kΩ	0.15V
2.5V ± 0.2V	V_{CC}	≦2ns	$V_{CC}/2$	$2\times V_{CC}$	30pF	500Ω	0.15V
3.3V ± 0.3V	3V	≦2.5ns	1.5V	6V	50pF	500Ω	0.3V
5V ± 0.5V	V_{CC}	≦2.5ns	$V_{CC}/2$	$2\times V_{CC}$	50pF	500Ω	0.3V



Voltage Waveform Propagation Delay Times

Inverting and Non Inverting Outputs

Notes: A. C_L includes probe and jig capacitance

B. All pulses and supplied at pulse repetition rate ≦ 10MHz

C. The Inputs are measured separately one transition per measurement

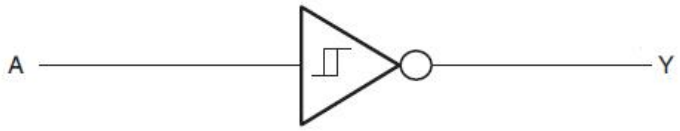
D. t_{PLH} and t_{PHL} are the same as t_{PD}

IC Operation Information

Basic Operation

The FLG74LVC2G14 single Schmitt-trigger inverter is designed for 1.65 V to 5.5 V operation and performs the Boolean function $Y=\overline{A}$. This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Function Block Diagram



Feature Description

• Wide operating voltage range.

-Operates from 1.65 V to 5.5 V.

• Allows down voltage translation.

• Inputs accept voltages to 5.5 V.

• Ioff feature allows voltages on the inputs and outputs when V_{CC} is 0 V.

Device Functional Table

INPUTS A	OUTPUT Y
H	L
L	H

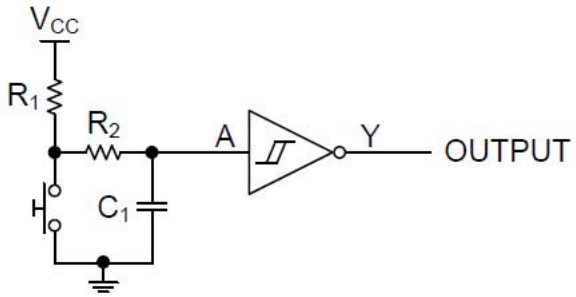
IC Application Information

Mechanical input elements, such as push buttons or rotary knobs, offer simple ways to interact with electronic systems. Typically, these elements have recoil or bouncing, where the mechanical element makes and breaks contact multiple times during human interaction. This bouncing can cause one or more repeated signals to be passed, triggering multiple actions when only a single input was intended. One potential solution to mitigating these multiple inputs is by utilizing a Schmitt-trigger to create a debounce circuit.

Typical Application

The input due to the push button switches multiple times, causing the output of a non Schmitt-trigger device to trigger multiple times, while the Schmitt-trigger input device with RC delay limits the output pulse to a single pulse desired by

the user. The separated positive and negative input voltage threshold values, see Figure , prevent multiple triggers from occurring.



Push Button Debounce Circuit Schematic

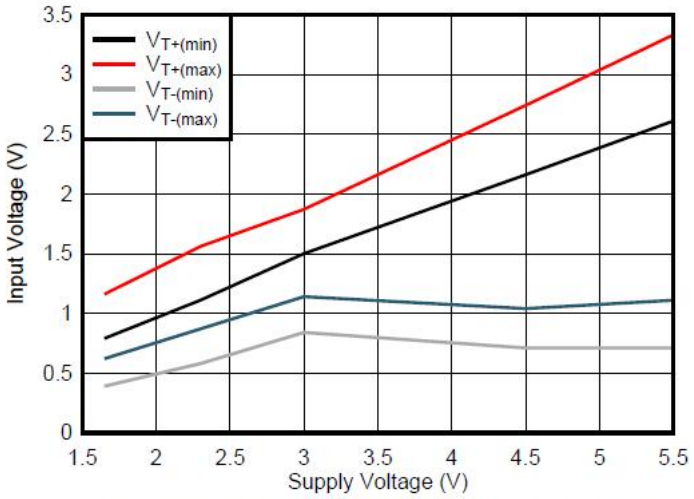
Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

Detailed Design Procedure

1. Recommended Input Conditions
   - – Rise time and fall time specs. See ($\Delta t/\Delta V$) in the Recommended Operating Conditions table.
   - – Specified high and low levels. See (V_{IH} and V_{IL}) in the Recommended Operating Conditions table.
   - – Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the Recommended Operating Conditions table at any valid V_{CC}.
2. Recommend Output Conditions
   - – Load currents should not exceed (I_O max) per output and should not exceed total current (continuous current through V_{CC} or GND) for the part. These limits are located in the Absolute Maximum Ratings table
   - – Outputs should not be pulled above V_{CC}.

Application Curves



Interpolated Threshold Voltages vs. V_{CC}

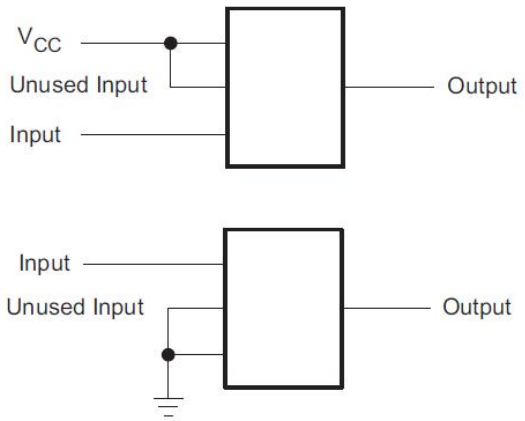
Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the Recommended Operating Conditions table.

Each Vcc pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF capacitor is recommended and if there are multiple Vcc pins then 0.01-µF or 0.022-µF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

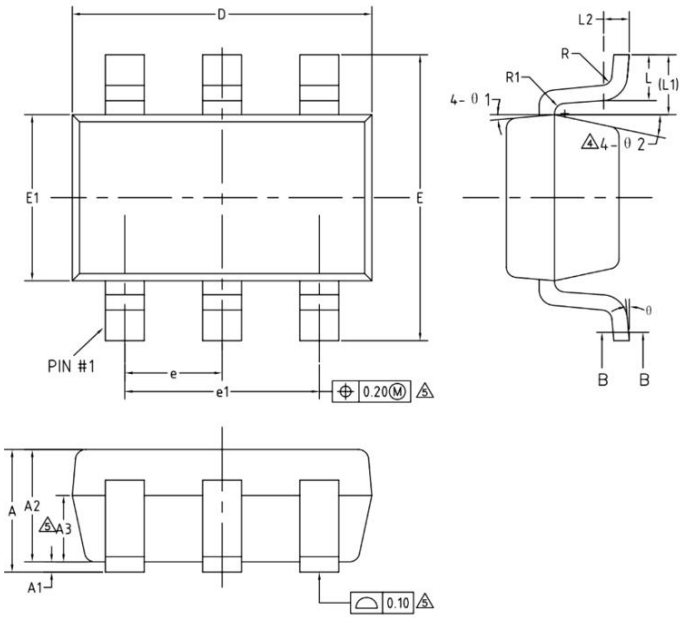
Layout Considerations

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input buffer gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or VCC whichever make more sense or is more convenient.



Package Information

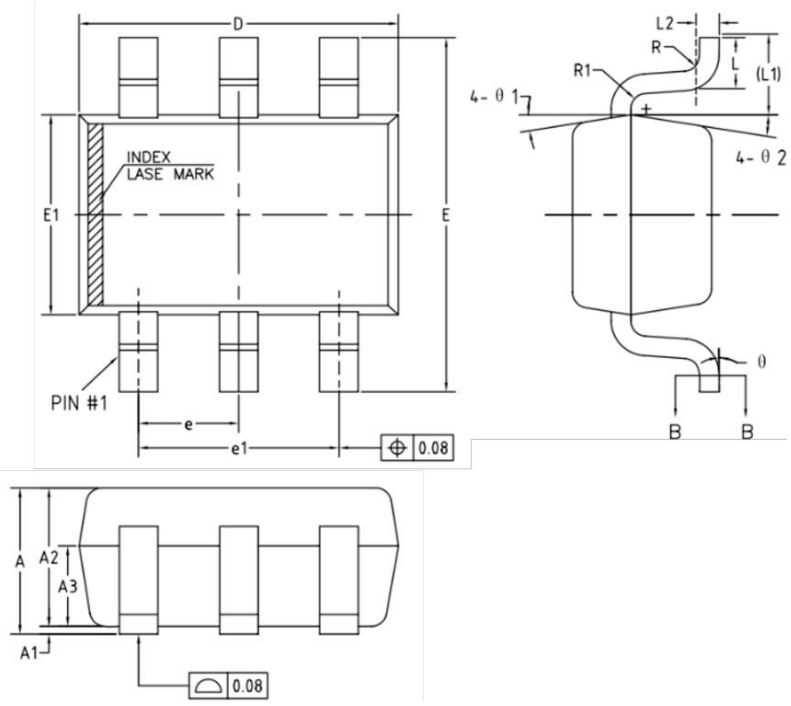
(1) Package Type:SOT23-6



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

	SYMBOL	MIN	NOM	MAX
	A	–	–	1.25
	A1	0	–	0.15
	A2	1.00	1.10	1.20
	A3	0.60	0.65	0.70
	b	0.36	–	0.50
	b1	0.36	0.38	0.45
	c	0.14	–	0.20
	c1	0.14	0.15	0.16
	D	2.826	2.926	3.026
	E	2.60	2.80	3.00
	E1	1.526	1.626	1.726
④	e	0.90	0.95	1.00
④	e1	1.80	1.90	2.00
	L	0.35	0.45	0.60
	L1		0.59REF	
	L2		0.25BSC	
③	R	0.10	–	–
③	R1	0.10	–	0.20
	θ	0°	–	8°
	θ1	3°	5°	7°
④	θ2	6°	–	14°

(2) Package Type: SC70-6



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.85	–	1.05
A1	0	–	0.10
A2	0.80	0.90	1.00
A3	0.47	0.52	0.57
2 b	0.22	–	0.29
b1	0.22	0.25	0.28
3 2 c	0.115	–	0.15
3 c1	0.115	0.13	0.14
D	2.02	2.07	2.12
E	2.20	2.30	2.40
E1	1.25	1.30	1.35
e	0.65BSC		
e1	1.30BSC		
L	0.28	0.33	0.38
L1	0.50REF		
L2	0.15BSC		
R	0.10	–	–
R1	0.10	–	0.25
θ	0°	–	8°
θ 1	6°	9°	12°
θ 2	6°	9°	12°

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