## Description

FEP24C02 is a standalone I²C compatible Serial EEPROM chip. The total memory array density is 2K bits, which is composed of 16 pages with 16 bytes per page.

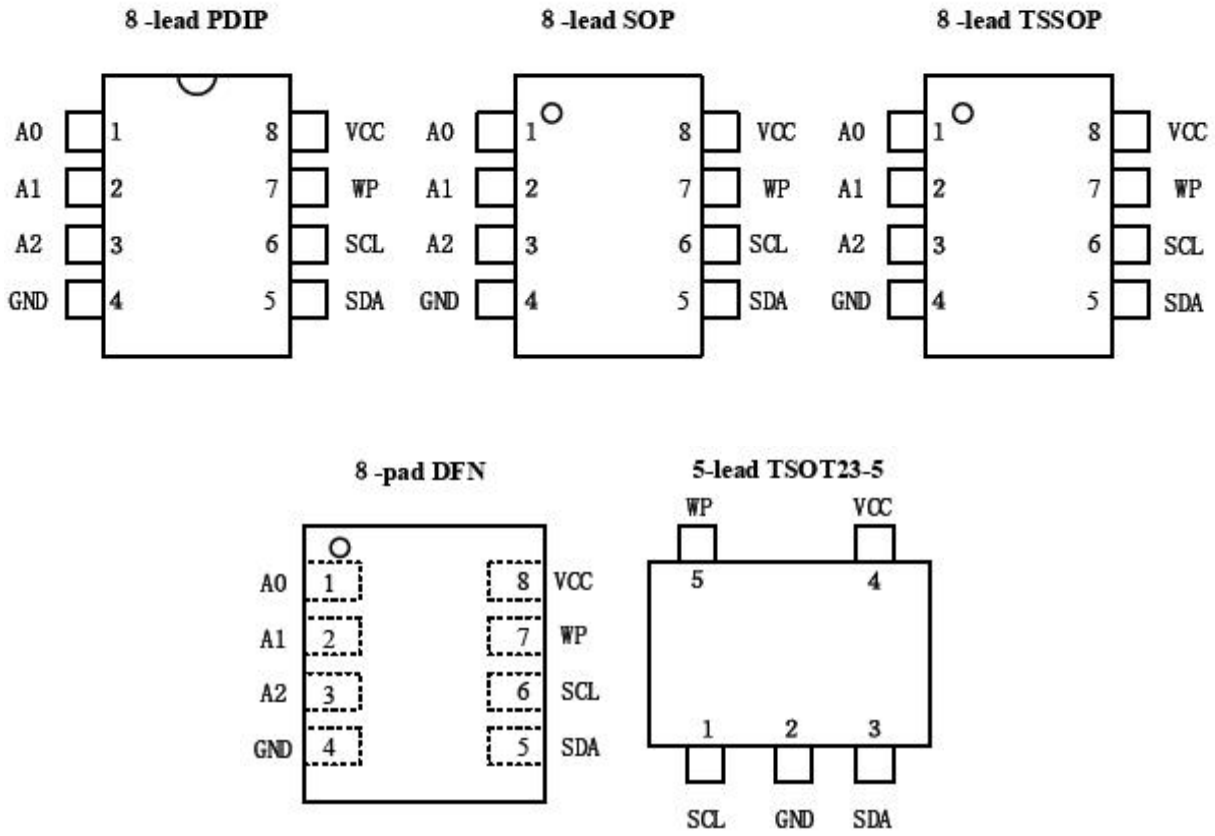
## Features

- Single supply voltage and high speed:
  - 1 MHz clock from 1.7 V to 5.5 V
- Operating Temperature range:
  - -40°C to +85°C
- Compatible with all I2C bus mode:
  - 100kHz
  - 400kHz,
  - 1MHz
- Memory Array:
  - 2Kbit EEPROM
  - 16 Pages
  - Page size: 16 byte
- Schmitt Trigger based noise filter for input noise suppression
- Current, Random and Sequential Read modes
- Write Operations:
- Ceramic Capacitor Stable
  - Byte write within 5 ms
  - Page write within 5 ms
  - Partial Page-writes support
  - Self-Timed Write Cycle
- Hardware write protection for the whole memory array
- High Reliability:
  - More than 1 million Write Endurance Cycles
  - More than 10 years Data Retention
- Package： SOP8, TSSOP8, UDFN8, PDIP8, SOT23-5

## Order information

| Mode | Package | Ordering Number | Packing Option |
|---|---|---|---|
| FEP24C02 | SOP8 | FEP24C02YSOP8G/TR | Tape and Reel |
| | TSSOP8 | FEP24C02YTSSOP8G/TR | Tape and Reel |
| | UDFN8 | FEP24C02YUDFN8G/TR | Tape and Reel |
| | PDIP8 | FEP24C02YPDIP8G/TR | Tape and Reel |
| | SOT23-5 | FEP24C02YSOT235G/TR | Tape and Reel |

## Pin Configuration




## PIN DESCRIPTION

Table 1 Pin Definition

| Pin No | Pin Name | I/O | Pin Function |
|---|---|---|---|
| 1 | A0 | I | Device Address Input. Internal Pull Down |
| 2 | A1 | I | Device Address Input. Internal Pull Down |
| 3 | A2 | I | Device Address Input. Internal Pull Down |
| 4 | GND | - | Ground |
| 5 | SDA | I/O | Serial Address, Data input and Data output(Open drain) |

| | | | |
|---|---|---|---|
| 6 | SCL | I | Serial Clock Input |
| 7 | WP | I | Write Protect Input. Internal Pull Down |
| 8 | VCC | - | Power Supply |

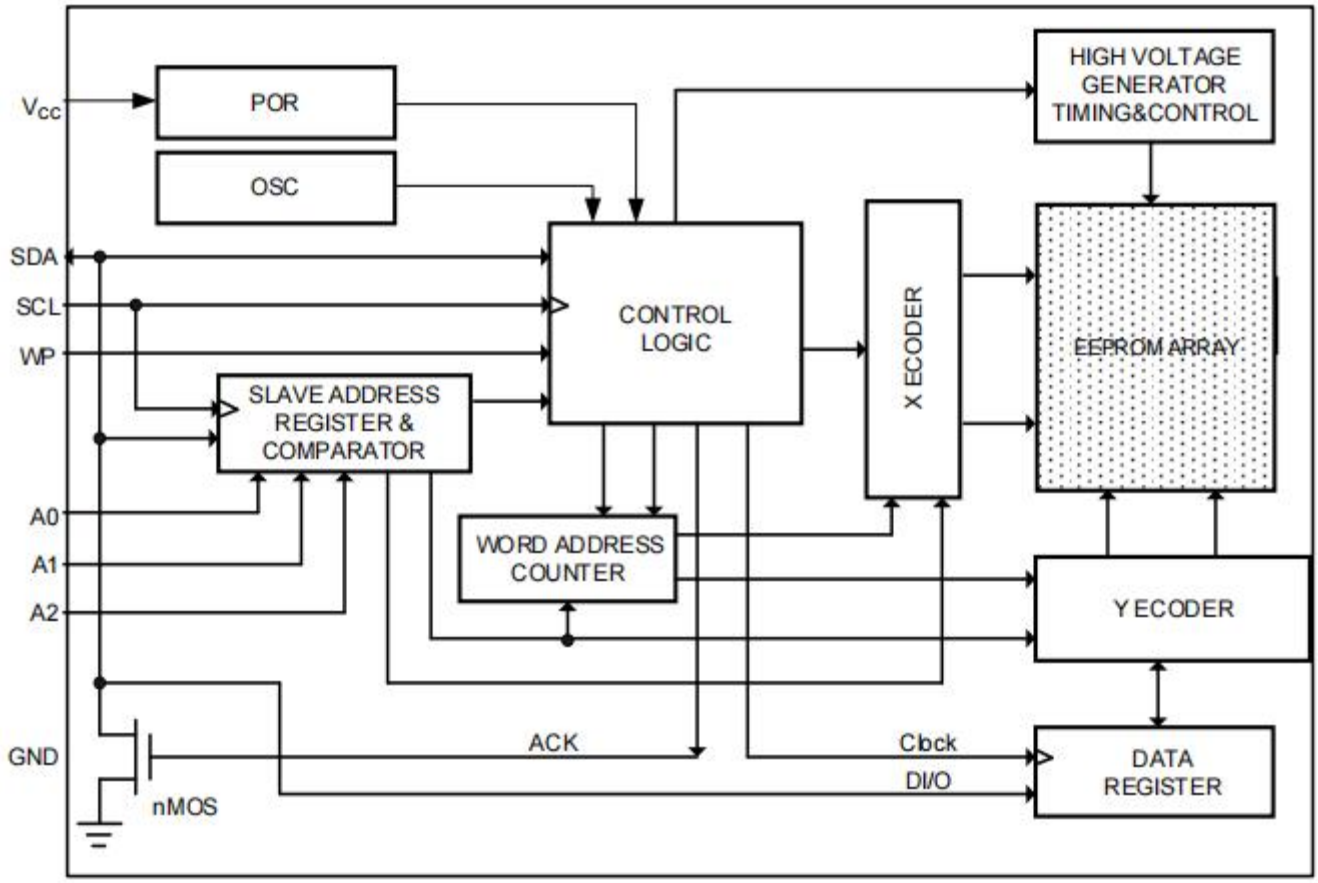
A0/A1/A2: The device address pin are used to select the device address. This pin can be directly connected to VCC or GND in any combination. When this pin is not connected (left floating), the input is read as zero.

SCL: The SCL pin is used to provide a clock to the device and to control the flow of data to and from the device. Command and input data present on the SDA pin is always latched in on the rising edge of SCL, while output data on the SDA pin is clocked out on the falling
edge of SCL.

SDA: The SDA pin is an open-drain bidirectional input/output pin used to serially transfer address and data to and from the device. The SDA pin must be pulled-high using an
external pull-up resistor and may be wire-ORed with any number of other open-drain or open-collector pins from other devices on the same bus.

WP: when the WP pin is connected to the VCC, the entire array becomes Write Protected. When this pin is not connected (left floating), the input is read as zero.

## Block Diagram



# Device Operation

## 1. POR Reset

There is an internal Power-On Reset (POR) circuit in chip to help prevent inadvertent operations during power-up and power down cycles. Before selecting the device and issuing protocol, a valid and stable supply voltage must be applied and no protocol should be issued to the device. The supply voltage must remain stable and valid until the end of the protocol transmission, and for a Write instruction, until the end of the internal write cycle.

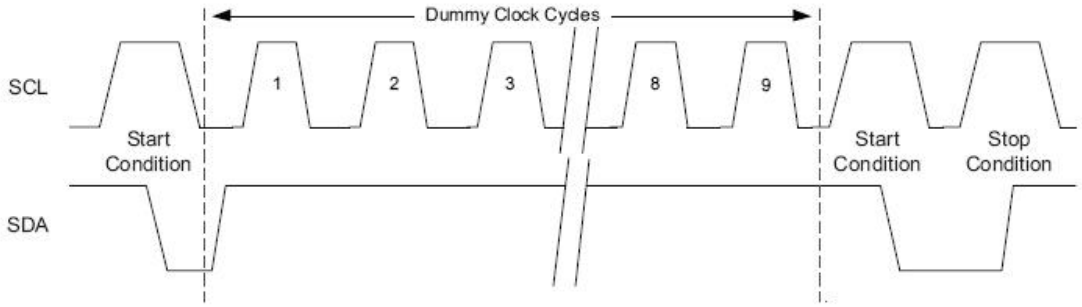
## 2. Software Reset

After an interruption in protocol, power loss, or system reset, any 2-wire part can be reset by following these steps:

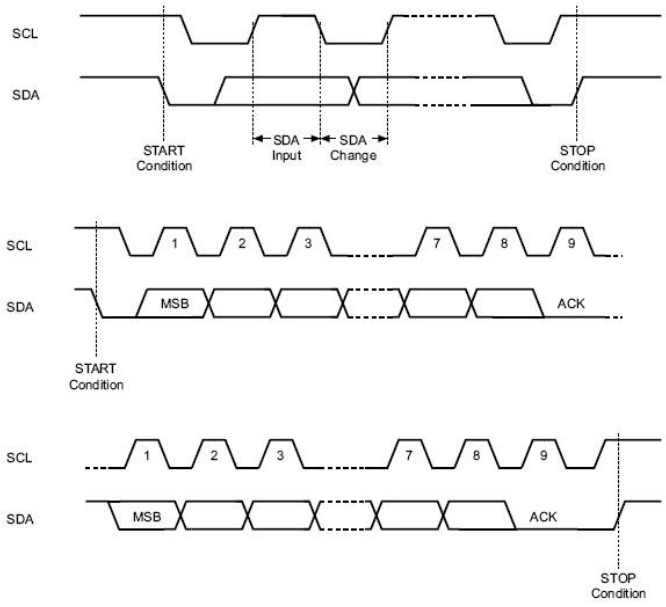
1. Create a Start condition.
2. Clock nine cycles.
3. Create another Start condition followed by a Stop condition.

The device will be ready for the next communication after the above steps have been completed.

The software reset will reset serial bus logic at lease to make sure SDA is released and enter standby mode with no ISB.




## 3. I2C Serial Interface




Serial Bus Protocol

### 3.1 Start Condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the High state. A Start condition must precede any data transfer command..

### 3.2 Data Input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL).

### 3.3 Acknowledge

The acknowledge bit is used to indicate a successful byte transfer. The no-acknowledge bit (NAK) is used to indicate the completion of a block read operation, or an attempt to modify a write-protected register.

### 3.4 Stop Condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven to High. A Stop condition terminates communication between the device and the bus master. A Stop condition at the end of a Write command triggers the internal EEPROM Write cycle.

### 3.5 Standby Mode

The chip enters into standby mode during one of the following conditions:

a) After Power-up, while no Op-code is sent;

b) After the completion of an operation and followed by the Stop signal, provided that the previous operation is not Write related;

c) After the completion of any internal write operations.

## 4. Device Address

To start communication, the bus master must initiate a Start condition. Following this, the bus master sends the device address byte with MSB first. The device address byte is comprised of a 4-bit device type identifier (DTI) followed by three software device address bits (SA2, SA1, and SA0) and a R/W bit, as described in Table 3.

Three device address bits are used to let up to eight devices can be connected on a single I2C Bus. The software device address bits must match their device address (A2, A1, A0). If a match occurs, the corresponding device gives an acknowledgment on serial data (SDA) during the 9th bit time. If the device does not acknowledge the device select code, the device de-selects itself from the bus, and goes into standby mode (therefore will not acknowledge the device select code).

The 8th bit is the Read/Write bit (RW). This bit is set to 1 for Read and 0 for Write operations.

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Memory Function | Device Type Identifier | | | | Software Device Address | | | (R/Wn) |
| Access EE Main Array | 1 | 0 | 1 | 0 | SA2 | SA1 | SA0 | 1/0 |

# 5. Write Operation

The chip supports single Byte Write and Page Write operations up to the maximum page size of 8 bytes in one operation. The only difference between a Byte Write and a Page Write operation is the amount of data bytes sent to the device. Regardless of whether a Byte Write or Page Write operation is performed, the internally self-timed write cycle will take the same amount of time to write the data to the addressed memory location(s).

## 5.1 Byte Write

Following the Start condition from the Master, the device type identifier, the device address bits and the R/W select bit (set to a Logic 0) are clocked onto the bus by the Master. The chip will respond with an ACK during the ninth clock cycle. Then the next byte transmitted by the Master is the 8-bit word address of the byte location to be written into the Serial EEPROM. After receiving an ACK, the Master transmits the data word to be programmed followed by an ACK from the chip. The Master ends the Write sequence with a Stop condition during the 10th clock cycle to initiate the internally self-timed write cycle. All inputs on SCL and SDA are ignored by the device during the write cycle and the device will not respond until the write cycle is complete. The Serial EEPROM will increment its internal address counter each time a byte is written.

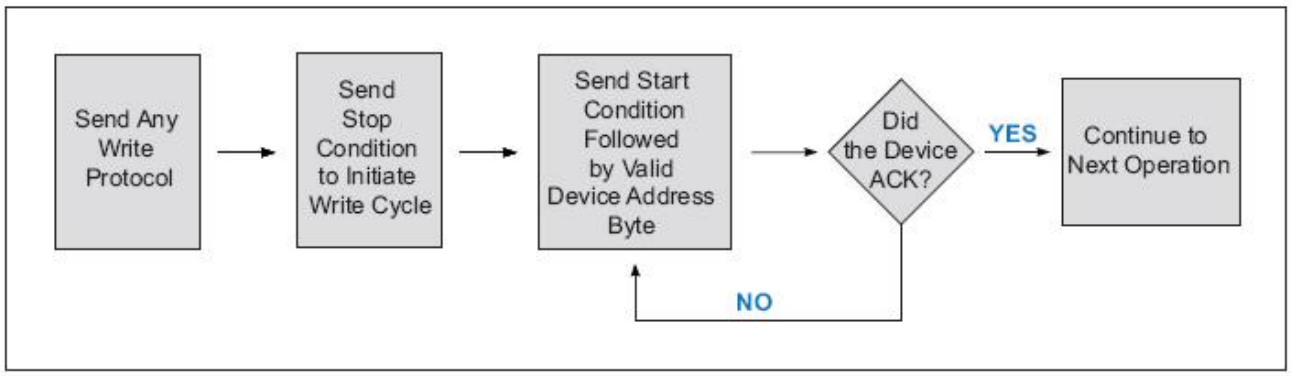
## 5.2 Page Write

A partial or full Page Write operation is initiated the same as a Byte Write operation except that the Master does not send a Stop condition after the first data word is clocked in. Instead, after the device has acknowledged receipt of the first data word, the Master can transmit up to 7more data words. The device will respond with an ACK after each data word is received. The Master must terminate the Page Write sequence with a Stop condition during the 10th clock cycle to start the write cycle. A Stop condition issued at any other clock cycle will not initiate the internally self-timed write cycle and the Write sequence will have to be repeated again.

When the internally generated word address reaches the page boundary, then the following data word is placed at the beginning of the same page. If more than one page data are transmitted to the device, the data word address will roll-over and the previous data will be overwritten. The address roll-over during a Write sequence is from the last byte of the current page to the first byte of the same page.

## 5.3 ACK Polling

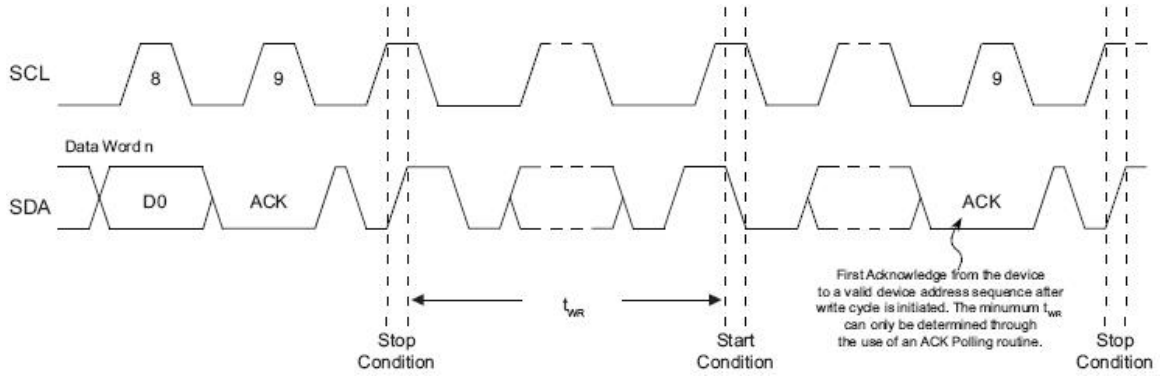
An ACK polling routine can be implemented to optimize time sensitive applications that prefer to know immediately when the Serial EEPROM write cycle has completed to start a subsequent operation.




ACK Polling

### 5.4 Write Cycle Timing

The length of the self-timed write cycle, or TWR, is defined as the amount of time from a valid Stop condition that begins the internal write sequence to the Start condition of the first device address byte sent to the chip that it subsequently responds to with an ACK.




Write Cycle Timing

## 6. Read Operation

All memory data Read operations are initiated by the Master transmitting a Start bit, a device type identifier of '1010', three software address bits (A2, A1, A0) that match their corresponding configurable device address (CDA2,CDA1,CDA0), and the R/W select bit with a Logic 1 state. In the following clock cycle, the device should respond with an ACK. Thesubsequent protocol depends on the type of Read operation desired.

Read operations are performed independent of the software protection state. The device hasan internal address counter which is incremented each time a byte is read.

### 6.1 Current Address Read

Following a Start condition, the Master only transmits the device address byte with the R/W select bit set to a Logic 1. The chip should respond with an ACK and then serially transmits the data word addressed by the internal address counter. The internal data word address counter maintains the last address accessed during the last Read or Write operation, incremented by one. This address stays valid between operations as long as power to the device is maintained. The address roll-over during a Read is from the last byte of the last page to the first byte of the first page of the addressed 256byte (depends on the current address setting).To end the command, the Master does not respond with an ACK but does generate a following Stop condition.

### 6.2 Random Read

A Random Read operation allows the Master to access any memory location in a random manner and requires a dummy write sequence to preload the starting data word address. To perform a Random Read, the device address byte and the word address byte are transmitted to chip as part of the dummy write sequence. Once the device address byte and data word address are clocked in and acknowledged by chip, the Master must generate another Start condition. The Master initiates a Current Address Read by sending another device address byte with the R/W select bit to a Logic 1. Then chip acknowledges the device address byte,increments its internal address counter and serially clocks out the first data word. The device will continue to transmit sequential data words as long as the Master continues to ACK each data word. To end the sequence, the Master responds with a NACK and a Stop condition.

### 6.3 Sequential Read

A Sequential Read operation is initiated in the same way as a Random Read operation, except after the chip transmits the first data word, the Master responds with an ACK (instead of a NACK followed by a Stop condition). As long as the chip receives an ACK, it will continue to increment the data word address and serially clock out the sequential data words. When the internal address counter is at the last byte of the last page, the data word address will roll-over from address 0000h, and the Sequential Read operation will continue. The Sequential Read operation is terminated when the Master responds with a NACK followed by a Stop condition.

### 6.4 Acknowledge in Read Mode

For all Read commands, the device waits, after each byte read, for an acknowledgment during the 9th bit time. If the bus master does not drive Serial Data (SDA) Low (NACK) during this time, the device terminates the data transfer and returns to an idle state to await the next valid START condition

## Initial Delivery State

The device is delivered with all the memory array bits set to 1.

## Absolute Maximum Ratings

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| VCC | Supply Voltage | -0.5 to + 6.5 | V |
| VN | Voltage on Input Pins | -0.5 to + 6.5 | V |
| TJ(max) | Maximum Junction Temperature | 150 | °C |
| Top | Operation Temperature | -40 to +85 | °C |
| Tstg | Storage Temperature | -65 to +150 | °C |

Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

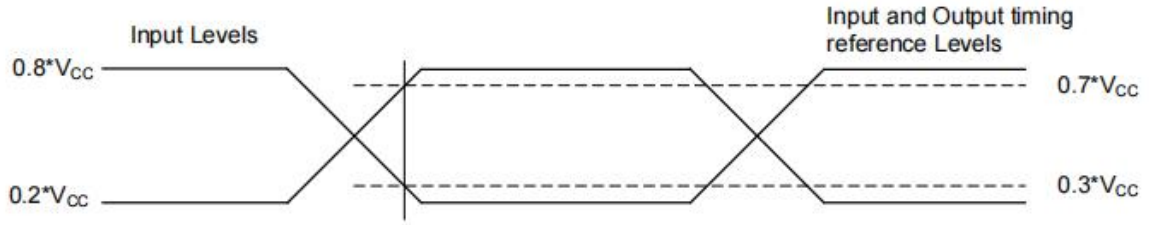
## Electrical Characteristics

- Capacitance

| Symbol | Parameter | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | -- | -- | 6 | pF |
| $C_{I/O}$ | Input / Output Capacitance | -- | -- | 8 | pF |

## ● AC Measurement Conditions

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| CL | Load capacitance | 100 | | pF |
| | Input rise and fall times | -- | 50 | ns |
| | Input levels | 0.2*VCC to 0.8*VCC | | V |
| | Input and output timing reference levels | 0.3*VCC to 0.7*VCC | | V |




## ● DC Electrical Characteristic

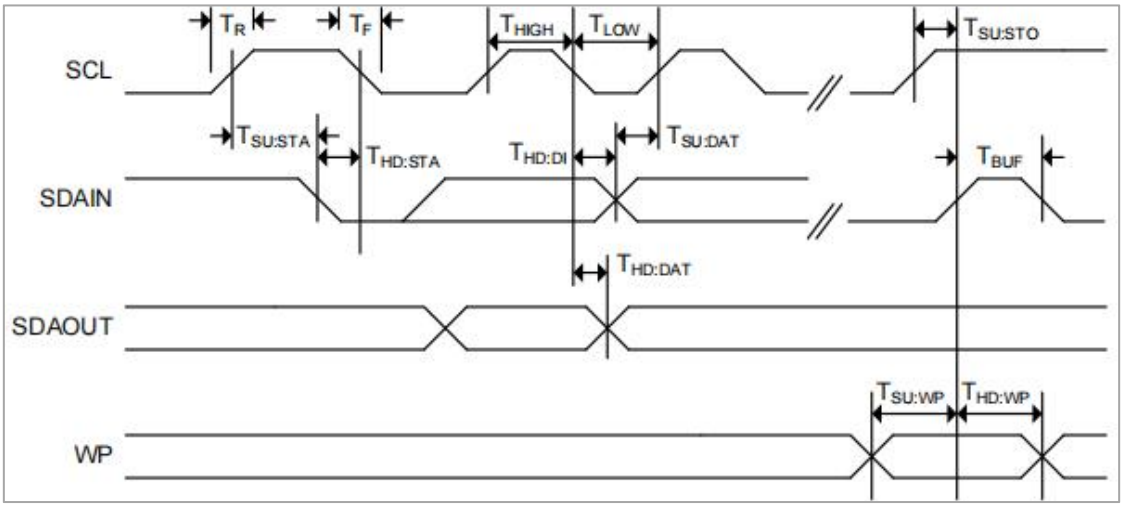
$V_{CC}$ = 1.7V to 5.5V, $T_{amb}$ = -40°C to +85°C, unless otherwise specified

| Symbol | Parameter | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage current(SCL,SDA) | $V_{IN}$=$V_{CC}$ or GND | -- | 2 | μA |
| $I_{LO}$ | Output leakage current | $V_{OUT}$=$V_{CC}$ or GND, SDA in Hi-Z | -- | 2 | μA |
| $I_{CC1}$ | Write Supply current | $V_{CC}$=5.5V, $f_C$=400KHz | -- | 1 | mA |
| $I_{CC2}$ | Read Supply current | $V_{CC}$=5.5V, $f_C$=400KHz | -- | 0.2 | mA |
| $I_{SB1}$ | Standby supply current | $V_{IN}$=$V_{CC}$, $V_{CC}$=3.0V | -- | 1 | μA |
| Vcc | Supply Voltage | | 1.7 | 5.5 | V |
| $V_{IH}$ | Input High Voltage | SCL, SDA | 0.7* $V_{CC}$ | $V_{CC}$+1 | V |
| $V_{IL}$ | Input Low Voltage | SCL, SDA | -0.5 | 0.3* $V_{CC}$ | V |
| $V_{OL1}$ | Output Low Voltage | Vcc=1.7V, SDA, $I_{OL}$ =0.2mA | -- | 0.2 | V |
| $V_{OL2}$ | | Vcc=3.0V, SDA $I_{OL}$ =2mA | -- | 0.4 | |

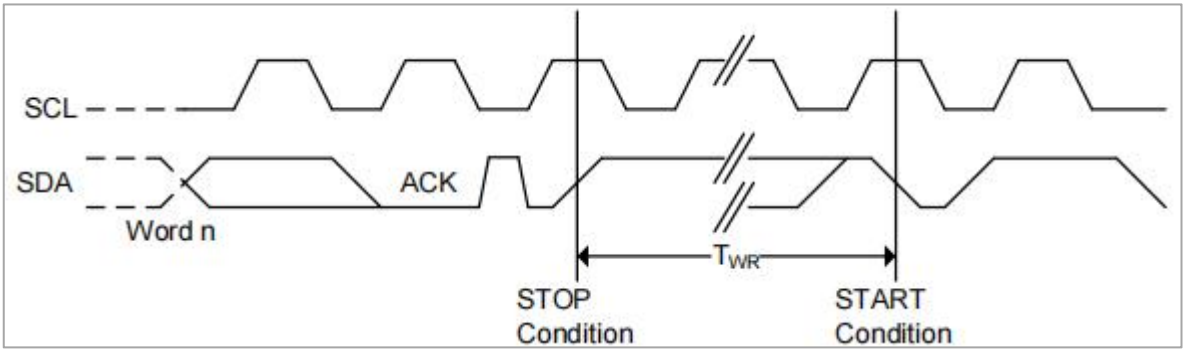
## ● AC Electrical Characteristic

$V_{CC}$ = 1.7V to 5.5V, $T_{amb}$ = -40~+85°C, unless otherwise specified

| Symbol | Parameter | VCC ≥1.7V | | | | Unit |
|---|---|---|---|---|---|---|
| | | 400KHz | | 1000KHz | | |
| | | Min. | Max. | Min. | Max. | |
| $F_{SCL}$ | SCL clock frequency | - | 400 | - | 1000 | kHz |
| $T_{LOW}$ | Low period of SCL clock | 1300 | | 400 | | ns |
| $T_{HIGH}$ | High period of SCL clock | 600 | | 400 | | ns |
| $T_{BUF}$ | Bus free time between a | 1300 | | 500 | | ns |
| $T_{SU;STA}$ | Start condition Setup time | 600 | | 260 | | ns |
| $T_{HD;STA}$ | Start condition Hold time | 600 | | 260 | | ns |
| $T_{SU;STO}$ | Stop condition Setup time | 600 | | 260 | | ns |
| $T_{SU;DAT}$ | Data In Setup time | 100 | | 50 | | ns |
| $T_{HD;DI}$ | Data In Hold time | 0 | | 0 | | ns |
| $T_{HD:DAT}$ | Data Out Hold Time | 100 | - | 0 | - | ns |
| $T_W$ | Write Cycle | | 5 | | 5 | ms |
| $T_R$ | Rise time of SDA | - | 300 | -- | 120 | ns |
| $T_F$ | Fall time of SDA | - | 300 | -- | 120 | ns |
| $T_N$ | Noise Suppression Time | - | 100 | - | 50 | ns |



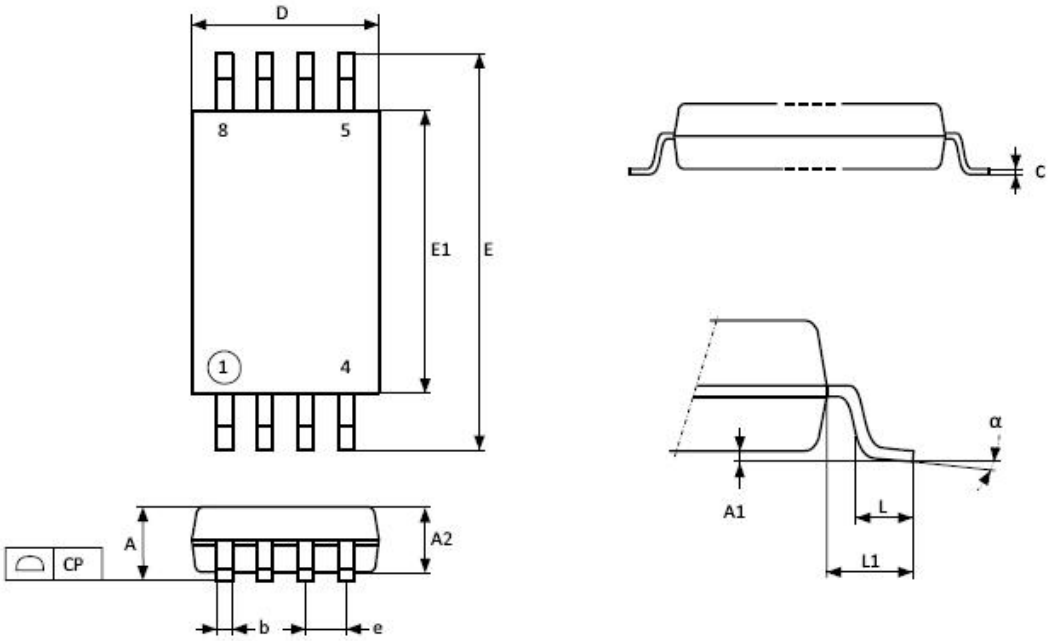

Bus Timing




Write Cycle Timing

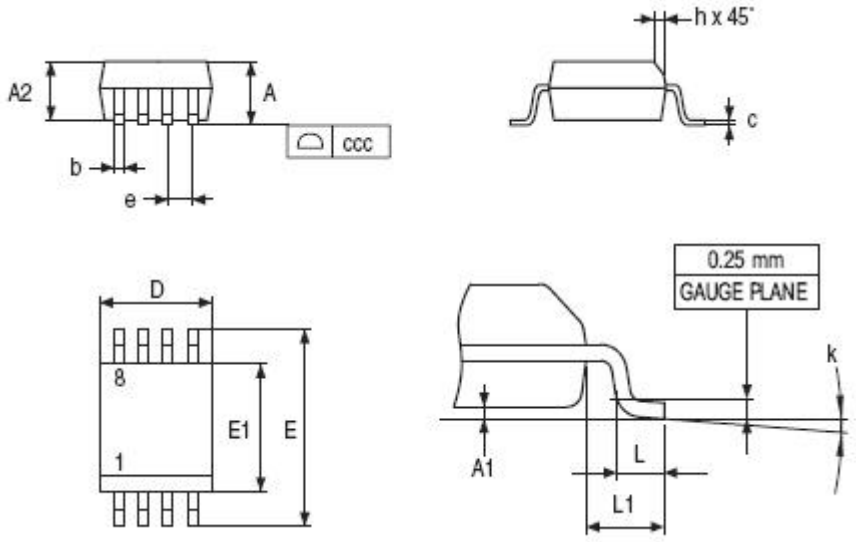
## Package Outline Dimensions(All dimensions in mm.)

(1) Package Type: TTSOP8



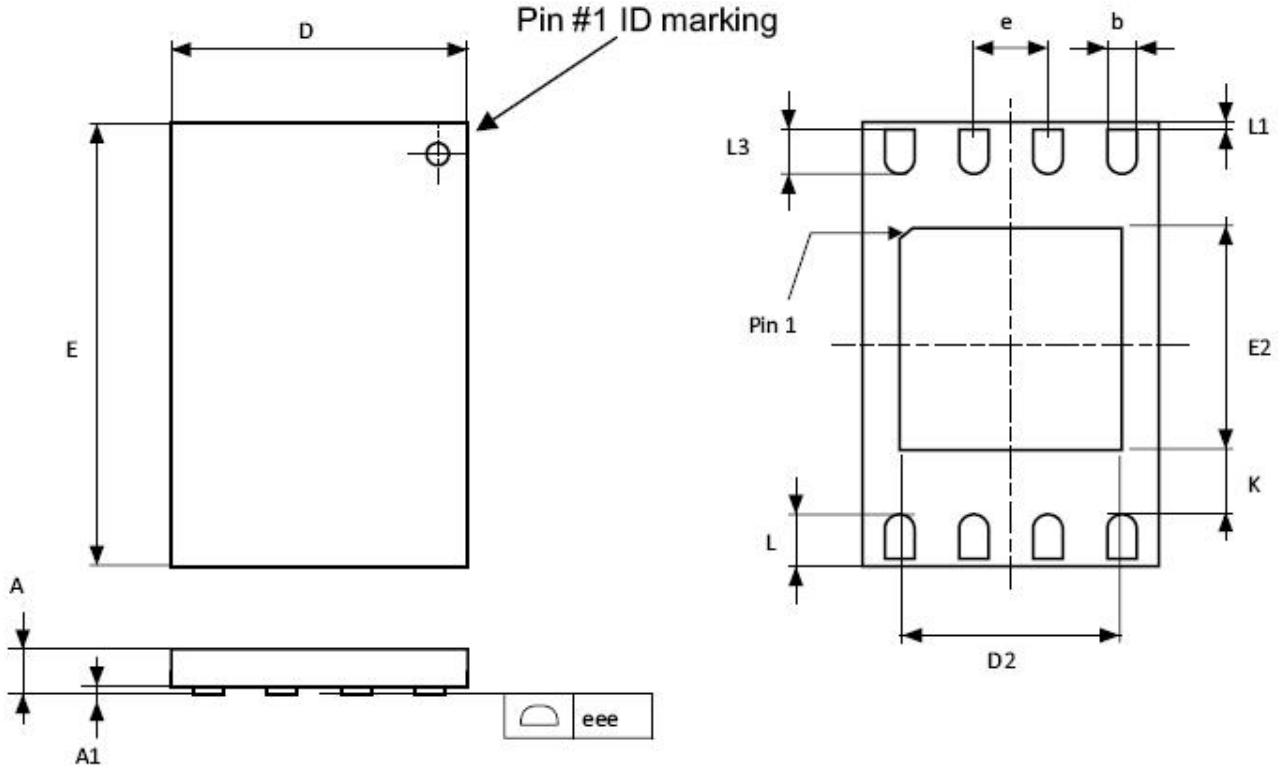

| Symbol | millimeters | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | - | - | 1.200 |
| A1 | 0.050 | - | 0.150 |
| A2 | 0.800 | 1.000 | 1.050 |
| b | 0.190 | - | 0.300 |
| c | 0.090 | - | 0.200 |
| CP | - | - | 0.100 |
| D | 2.900 | 3.000 | 3.100 |
| e | - | 0.650 | - |
| E | 6.200 | 6.400 | 6.600 |
| E1 | 4.300 | 4.400 | 4.500 |
| L | 0.450 | 0.600 | 0.750 |
| L1 | - | 1.000 | - |
| α | 0° | - | 8° |

(2) Package Type: SOP8



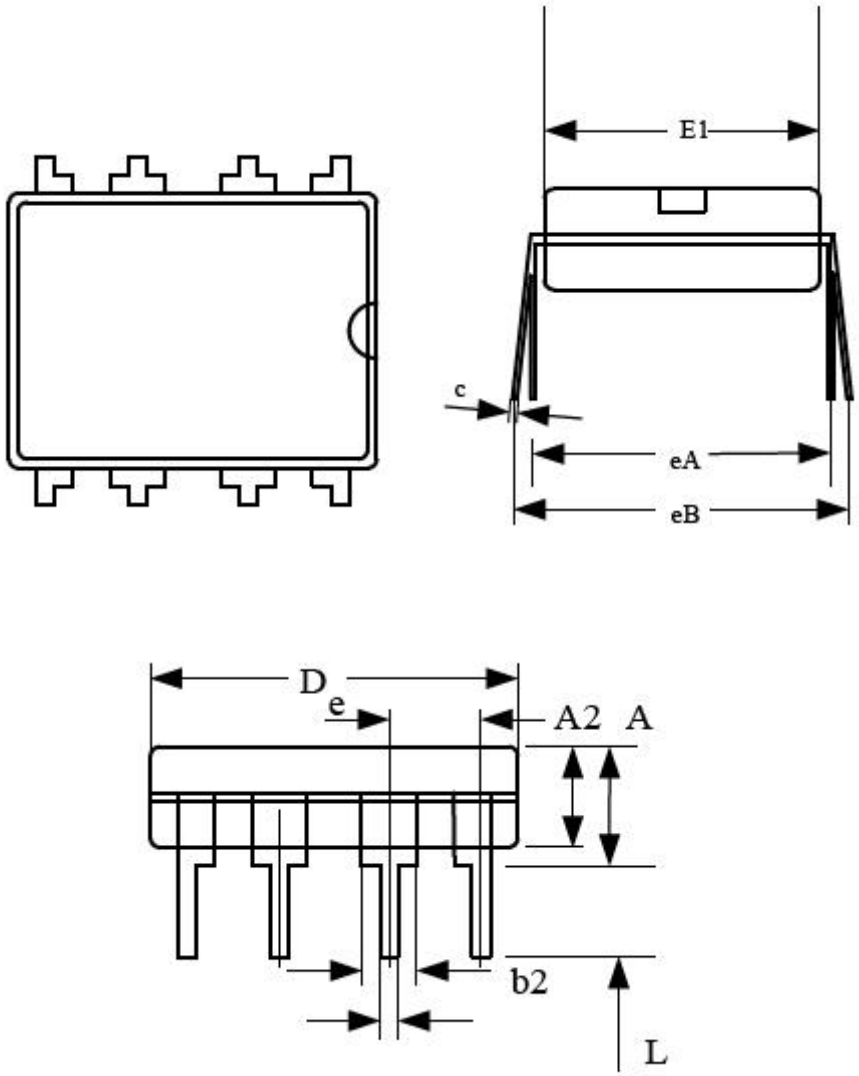

| Symbol | millimeters | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | - | - | 1.750 |
| A1 | 0.100 | - | 0.250 |
| A2 | 1.250 | - | - |
| b | 0.280 | - | 0.480 |
| c | 0.170 | - | 0.230 |
| D | 4.800 | 4.900 | 5.000 |
| E | 5.800 | 6.000 | 6.200 |
| E1 | 3.800 | 3.900 | 4.000 |
| e | - | 1.270 | - |
| h | 0.250 | - | 0.500 |
| k | 0° | - | 8° |
| L | 0.400 | - | 1.270 |
| L1 | - | 1.040 | - |
| ccc | - | - | 0.100 |

(3) Package Type: UDFN8



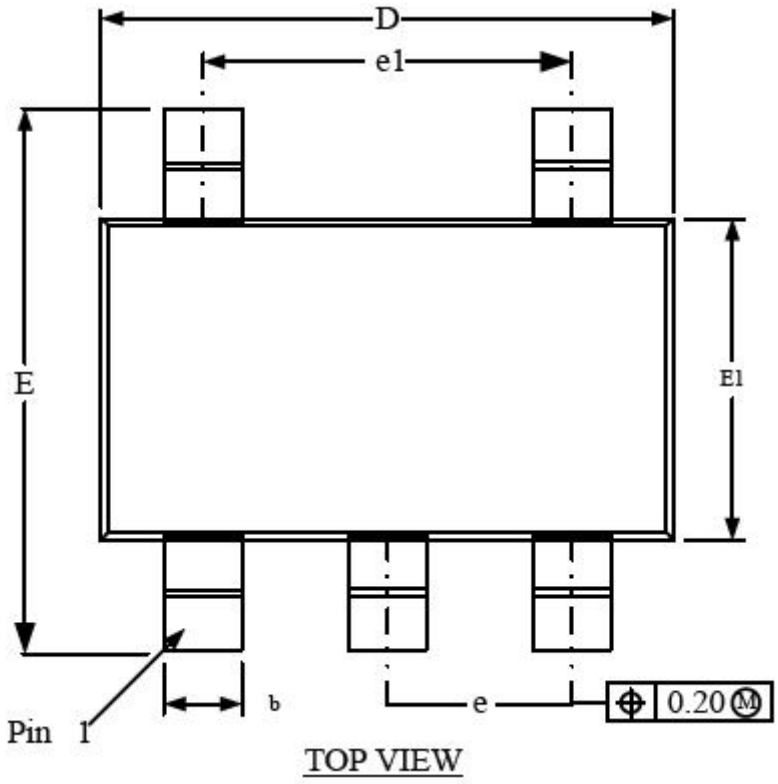

| Symbol | millimeters | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | 0.450 | 0.550 | 0.600 |
| A1 | 0.000 | 0.020 | 0.050 |
| b | 0.200 | 0.250 | 0.300 |
| D | 1.900 | 2.000 | 2.100 |
| D2 | 1.200 | - | 1.600 |
| E | 2.900 | 3.000 | 3.100 |
| E2 | 1.200 | - | 1.600 |
| e | - | 0.500 | - |
| K | 0.300 | - | - |
| L | 0.300 | - | 0.500 |
| L1 | - | - | 0.150 |
| L3 | 0.300 | - | - |
| eee(2) | 0.080 | - | - |

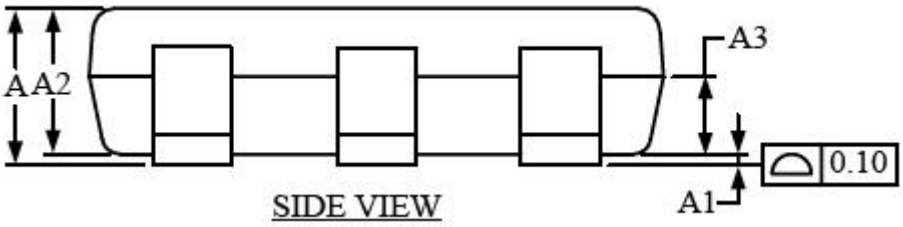
(4) Package Type: PDIP8




| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 3.60 | 3.80 | 4.00 |
| A2 | 3.20 | 3.30 | 3.40 |
| b | 0.44 | - | 0.53 |
| b2 | | 1.52BSC | |
| c | 0.24 | - | 0.32 |
| D | 9.05 | 9.25 | 9.45 |
| E1 | 6.15 | 6.35 | 6.55 |
| e | | 2.54BSC | |
| eA | | 7.62BSC | |
| eB | 7.62 | - | 9.30 |
| L | | 3.00BSC | |

(5) Package Type: SOT23-5




| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | - | - | 0.90 |
| A1 | 0.00 | - | 0.15 |
| A2 | 0.65 | 0.75 | 0.85 |
| A3 | 0.35 | 0.40 | 0.45 |
| c | 0.14 | - | 0.20 |
| c1 | 0.14 | 0.15 | 0.16 |
| D | 2.85 | 2.95 | 3.05 |
| E | 2.65 | 2.80 | 2.95 |
| E1 | 1.60 | 1.65 | 1.70 |
| e | 0.90 | 0.95 | 1.00 |
| e1 | 1.80 | 1.90 | 2.00 |
| L | 0.30 | 0.45 | 0.60 |
| L1 | 0.575REF | | |
| L2 | 0.258BSC | | |
| R | - | - | 0.25 |
| R1 | - | - | 0.25 |
| Θ | 0° | - | 8° |
| Θ1 | 3° | 5° | 7° |
| Θ2 | 10° | 12° | 14° |