1. Description

The FEP24C256 is an industrial standard electrically erasable programmable read only memory (EEPROM) device that utilizes the industrial standard 2-wire interface for communications. The FEP24C256 contains a memory array of 256K bits (32768x8), which is organized in 64-byte per page.

The EEPROM operates in a wide voltage range from 1.7Vto 5.5V, which fits most application . The product provides low-power operations and low standby current. The device is offered in Lead-free, RoHS, halogen free or Green package. The available package types are 8-pin SOIC, TSSOP, UDFN, MSOP.

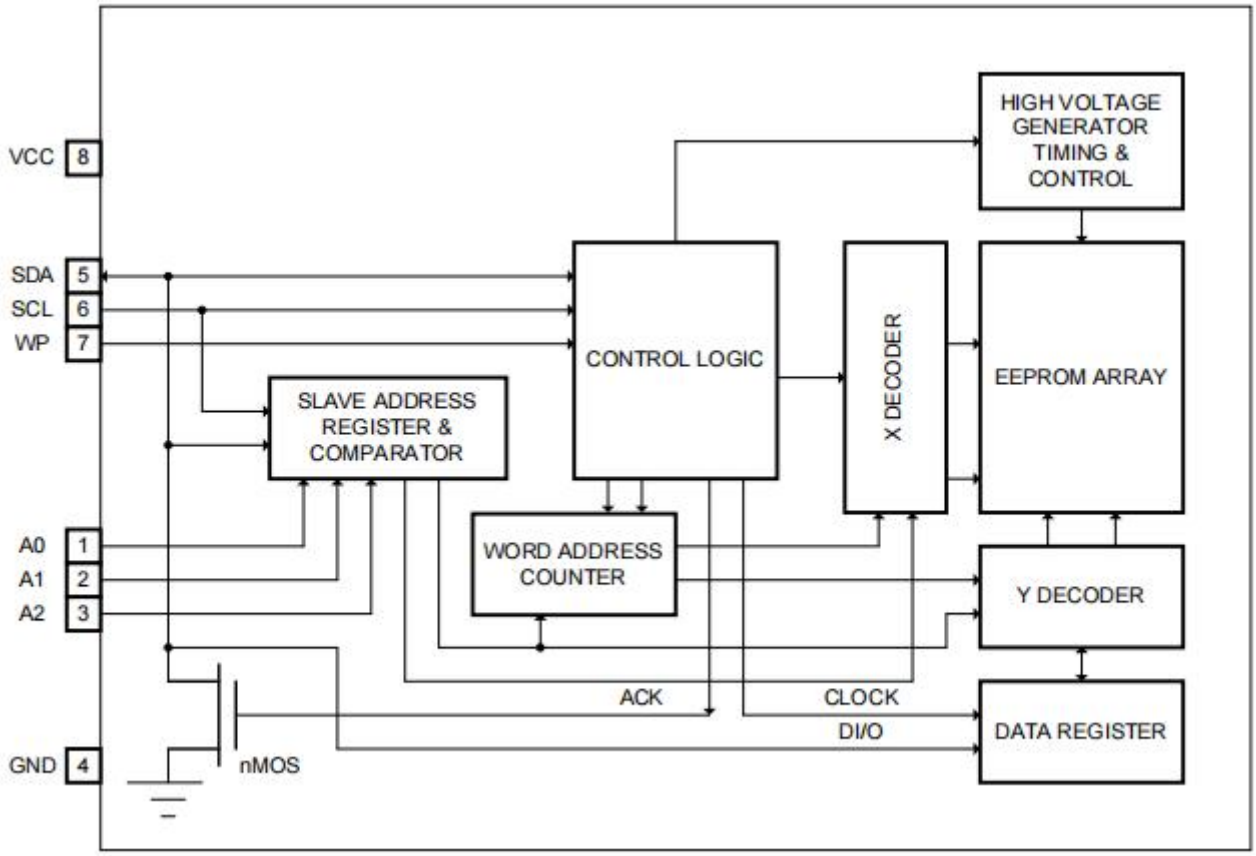
The FEP24C256 is compatible to the standard 2-wire bus protocol. The simple bus consists of Serial Clock (SCL) and Serial Data (SDA) signals. Utilizing such bus protocol, a Master device, such as a microcontroller, can usually control one or more Slave devices, alike this FEP24C256. The bit stream over the SDA line includes a series of bytes, which identifies a particular Slave device, an instruction, an address within that Slave device, and a series of data, if appropriate. The FEP24C256 also has a Write Protect function via WP pin to cease from over-writing the data stored inside the memory array.

In order to refrain the state machine from entering into a wrong state during power-up sequence or a power toggle off-on condition, a power on reset circuit is embedded. During power-up, the device does not respond to any instructions until the supply voltage (V_{CC}) has reached an acceptable stable level above the reset threshold voltage. Once V_{CC} passes the power on reset threshold, the device is reset and enters into the Standby mode. This would also avoid any inadvertent Write operations during power-up stage. During power-down process, the device will enter into standby mode, once V_{CC} drops below the power on reset threshold voltage. In addition, the device will be in standby mode after receiving the Stop command, provided that no internal write operation is in progress. Nevertheless, it is illegal to send a command unless the V_{CC} is within its operating level.

2. Features

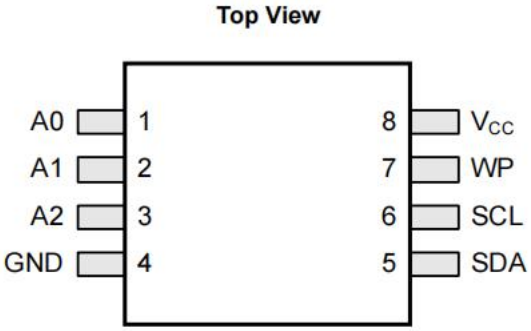
- Two-Wire Serial Interface, I^2C^{TM} Compatible
  - Bi-directional data transfer protocol
- Wide-voltage Operation
  - V_{CC} = 1.7V to 5.5V
- Speed: 1 MHz (1.7V~5.5V)
- Standby current (max.): 1 μA, 1.7V
- Read current (max.): 0.5 mA, 5.5V
- Write current (max.):0.8 mA, 5.5V
- Hardware Data Protection
  - Write Protect Pin
- Sequential & Random Read Features
- Memory organization: 256Kb (32768x 8)
- Page Size: 64 bytes
- Page write mode
  - Partial page writes allowed
- Self timed write cycle: 5 ms (max.)
- Noise immunity on inputs, besides Schmitt trigger
- High-reliability
  - Endurance: 1 million cycles
  - Data retention: 100 years
- ESD Protection > 7500V
- Industrial grade
- Packages: SOIC, TSSOP, UDFN, MSOP,PDIP
- Lead-free, RoHS, Halogen free,Green

3. Functional Block Diagram

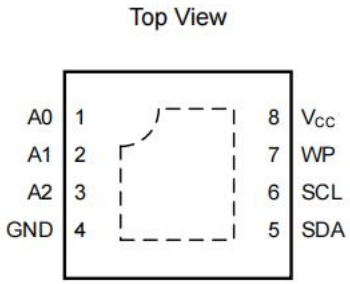


4. Pin Configuration

4.1. 8-Pin SOIC, TSSOP, MSOP and PDIP



4.2. 8-Lead UDFN



4.3. Pin Definition

Pin No.	Pin Name	I/O	Definition
1	A0	I	Device Address Input
2	A1	I	Device Address Input
3	A2	I	Device Address Input
4	GND	-	Ground
5	SDA	I/O	Serial Address, Data input and Data output
6	SCL	I	Serial Clock Input
7	WP	I	Write Protect Input
8	VCC	-	Power Supply

4.4. Pin Descriptions

SCL

This input clock pin is used to synchronize the data transfer to and from the device.

SDA

The SDA is a bi-directional pin used to transfer addresses and data into and out of the device. The SDA pin is an open drain output and can be wired with other open drain or open collector outputs. However, the SDA pin requires a pull-up resistor connected to the power supply.

WP

WP is the Write Protect pin. While the WP pin is connected to the power supply of FEP24C256, the entire array becomes Write Protected (i.e. the device becomes Read only). When WP is tied to Ground or left floating, the normal write operations are allowed.

A0, A1, A2

The A0, A1 and A2 are the device address inputs.

Typically, the A0, A1, and A2 pins are for hardware addressing and a total of 8 devices can be connected on a single bus system. When A0, A1, and A2 are left floating, the inputs are defaulted to zero.

VCC

Supply voltage

GND

Ground of supply voltage

5. Device Operation

The FEP24C256 serial interface supports communications using the standard 2-wire bus protocol, such as I^2C.

5.1 2-WIRE Bus

The two-wire bus is defined as Serial Data (SDA), and Serial Clock (SCL). The protocol defines any device that sends data onto the SDA bus as a transmitter, and the receiving devices as receivers. The bus is controlled by Master device that generates the SCL, controls the bus access, and generates the Start and Stop conditions. The FEP24C256 is the Slave device.

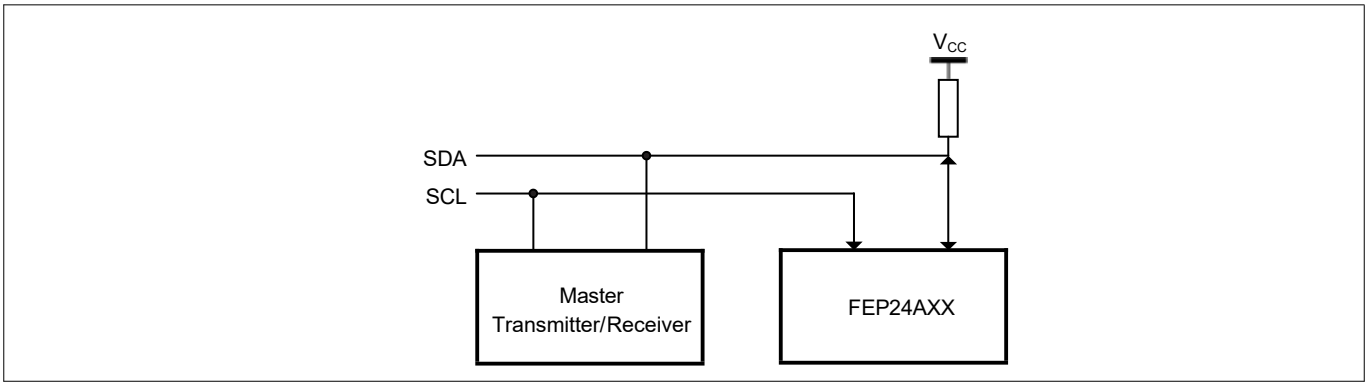


Figure 1.TypicalSystem Bus Configuration

5.2 The Bus Protocol

Data transfer may be initiated only when the bus is not busy. During a data transfer, the SDA line must remain stable whenever the SCL line is high. Any changes in the SDA line while the SCL line is high will be interpreted as a Start or Stop condition.

The state of the SDA line represents valid data after a Start condition. The SDA line must be stable for the duration of the High period of the clock signal. The data on the SDA line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a Start condition and terminated by a Stop condition.

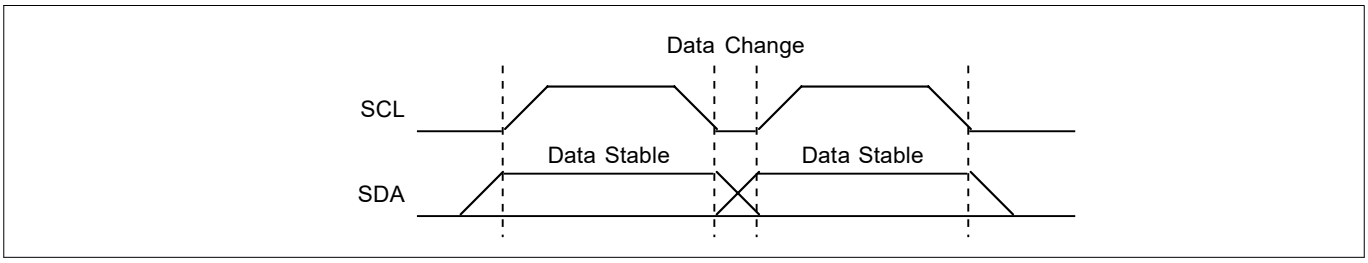


Figure2.Data Validity Protocol

5.3 Start Condition

The Start condition precedes all commands to the device and is defined as a High to Low transition of SDA when SCL is High. The EEPROM monitors the SDA and SCL lines and will not respond until the Start condition is met.

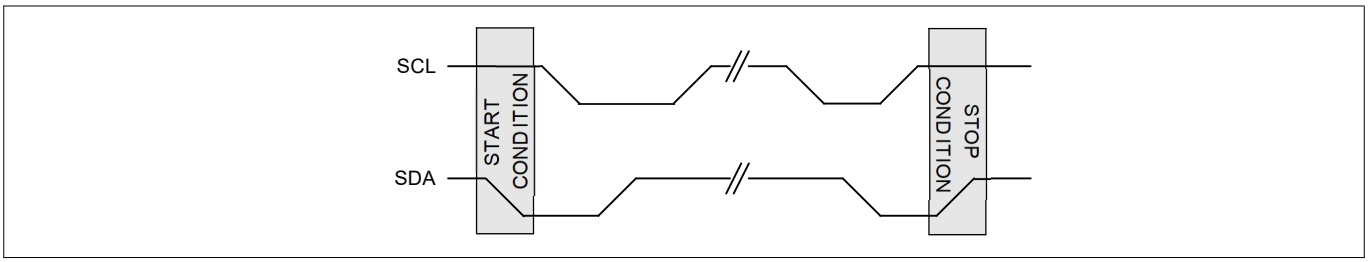


Figure3.Start and Stop Conditions

5.4 Stop Condition

The Stop condition is defined as a Low to High transition of SDA when SCL is High. All operations must end with a Stop condition.

5.5 Acknowledge

After a successful data transfer, each receiving device is required to generate an ACK. The Acknowledging device pulls down the SDA line.

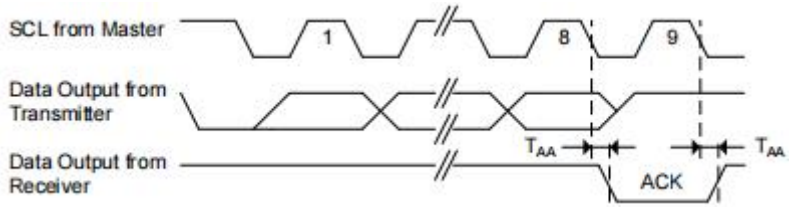


Figure 4.Output Acknowledge

5.6 Reset

The FEP24C256 contains a reset function in case the 2-wire bus transmission on is accidentally interrupted (e.g. a power loss),or needs to be terminated mid-stream. The reset is initiated when the Master device creates a Start condition. To do this, it may be necessary for the Master device to monitor the SDA line while cycling the SCL up to nine times. (For each clock signal transition to High, the Master checks for a High level on SDA.)

5.7 Standby Mode

While in standby mode, the power consumption is minimal. The FEP24C256 enters into standby mode during one of the following conditions: a) After Power-up, while no Op-code is sent; b) After the completion of an operation and followed by the Stop signal, provided that the previous operation is not Write related; or c) After the completion of any internal write operations.

5.8 Device Addressing

The Master begins a transmission on by sending a Start condition, then sends the address of the particular Slave devices to be communicated. The Slave device address is 8 bits format as shown in Figure 5.

The four most significant bits of the Slave address are fixed (1010) for FEP24C256.

The next three bits, A2, A1 and A0, of the Slave address are specifically related to EEPROM. Up to eight FEP24C256 units can be connected to the 2-wire bus.

The last bit of the Slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, Read operation is selected. While it is set to 0, Write operation is selected.

After the Master transmits the Start condition and Slave address byte appropriately, the associated 2-wire Slave device, FEP24C256, will respond with ACK on the SDA line. Then FEP24C256 will pull down the SDA on the ninth clock cycle, signaling that it received the eight bits of data.

The FEP24C256 then prepares for a Read or Write operation by monitoring the bus.

Bit	7	6	5	4	3	2	1	0
	1	0	1	0	A2	A1	A0	R / $\overline{W}$

Note: FEP24C256 does not support the address 1001 100xb. x=R/W.

Figure5.Slave Address

5.9 Write Operation

5.9.1 Byte Write

In the Byte Write mode, the Master device sends the Start condition and the Slave address information (with the R/W set to Zero) to the Slave device. After the Slave generates an ACK, the Master sends the byte address that is to be written into the address pointer of the FEP24C256. After receiving another ACK from the Slave, the Master device transmits the data byte to be written into the address memory location. The FEP24C256 acknowledges once more and the Master generates the Stop condition, at which time the device begins its internal programming cycle. While this internal cycle is in progress, the device will not respond to any request from the Master device.

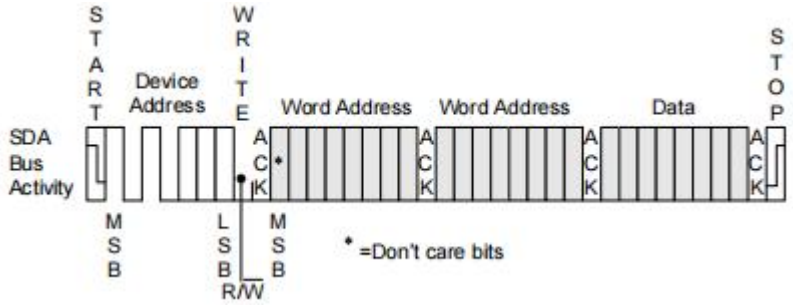


Figure 6.Byte Write

5.9.2 Page Write

The FEP24C256 is capable of 64-byte Page-Write operation. A Page-Write is initiated in the same manner as a Byte Write, but instead of terminating the internal Write cycle after the first data word is transferred, the Master device can transmit up to 63 more bytes. After the receipt of each data word, the EEPROM responds immediately with an ACK on SDA line, and the six lower order data word address bits are internally incremented by one, while the higher order bits of the data word address remain constant. If a byte address is incremented from the last byte of a page, it returns to the first byte of that page. If the Master device should transmit more than 64 bytes prior to issuing the Stop condition, the address counter will "roll over," and the previously written data will be overwritten. Once all 64 bytes are received and the Stop condition has been sent by the Master, the internal programming cycle begins. At this point, all received data is written to the FEP24C256 in a single Write cycle. All inputs are disabled until completion of the internal Write cycle.

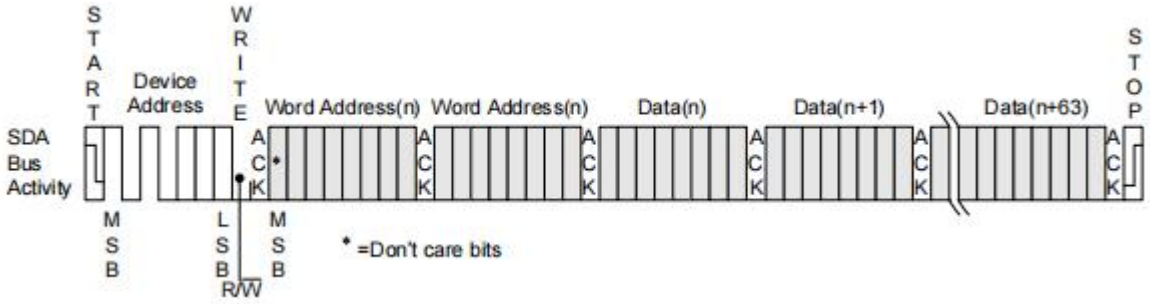


Figure 7.Page Write

5.9.3 Acknowledge (ACK) Polling

The disabling of the inputs can be used to take advantage of the typical Write cycle time. Once the Stop condition is issued to indicate the end of the host's Write operation, the FEP24C256 initiates the internal Write cycle. ACK polling can be initiated immediately. This involves issuing the Start condition followed by the Slave address for a Write operation. If the EEPROM is still busy with the Write operation, no ACK will be returned. If the FEP24C256 has completed the Write operation, an ACK will be returned and the host can then proceed with the next Read or Write operation.

5.10 Read Operation

Read operations are initiated in the same manner as Write operations, except that the (R/W) bit of the Slave address is set to "1" . There are three Read operation options: current address read, random address read and sequential read.

5.10.1 Current Address Read

The FEP24C256 contains an internal address counter which maintains the address of the last byte accessed, incremented by one. For example, if the previous operation is either a Read or Write operation addressed to the address location n, the internal address counter would increment to address location n+1. When the EEPROM receives the Slave Addressing Byte with a Read operation (R/W bit set to "1"), it will respond an ACK and transmit the 8-bit data byte stored at address location n+1. The Master should not acknowledge the transfer but should generate a Stop condition so the FEP24C256 discontinues transmission. If 'n' is the last byte of the memory, the data from location '0' will be transmitted. (Refer to Figure 8. Current Address Read Diagram.)

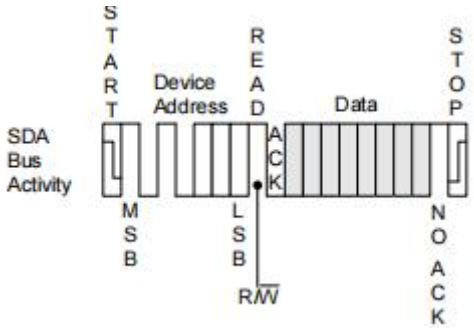


Figure8.Current Address Read

5.10.2 Random Address Read

Selective Read operations allow the Master device to select at random any memory location for a Read operation. The Master device first performs a 'dummy' Write operation by sending the Start condition, Slave address and byte address of the location it wishes to read. After the FEP24C256 acknowledges the byte address, the Master device resends the Start condition and the Slave address, this time with the R/W bit set to one. The EEPROM then responds with itsACK and sends the data requested. The Master device does not send an ACK but will generate a Stop condition. (Refer to Figure 9. Random Address Read Diagram.)

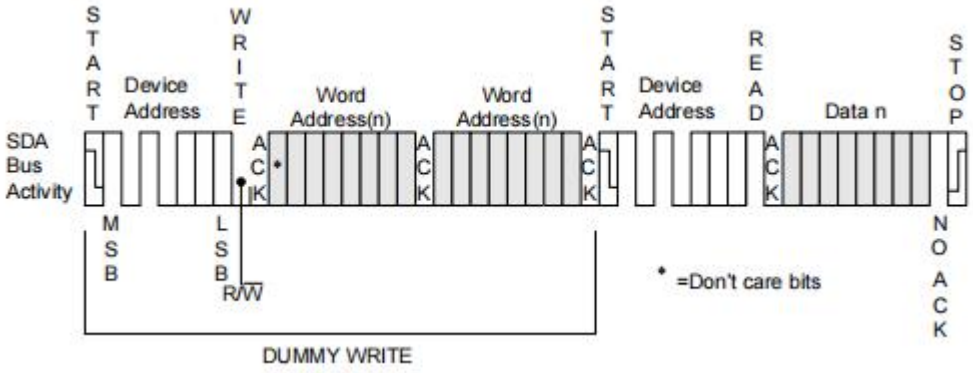


Figure 9. Random Address Read

5.10.3 Sequential Read

Sequential Reads can be initiated as either a Current Address Read or Random Address Read. After the FEP24C256 sends the initial byte sequence, the Master device now responds with an ACK indicating it requires additional data from the FEP24C256. The EEPROM continues to output data for each ACK received. The Master device terminates the sequential Read operation by pulling SDA High (no ACK) indicating the last data byte to be read, followed by a Stop condition. The data output is sequential, with the data from address n followed by the data from address n+1, n+2 ... etc. The address counter increments by one automatically, allowing the entire memory contents to be serially read during sequential Read operation. When the memory address boundary of the array is reached, the address counter “rolls over” to address 0, and the device continues to output data. (Refer to Figure 10. Sequential Read Diagram).

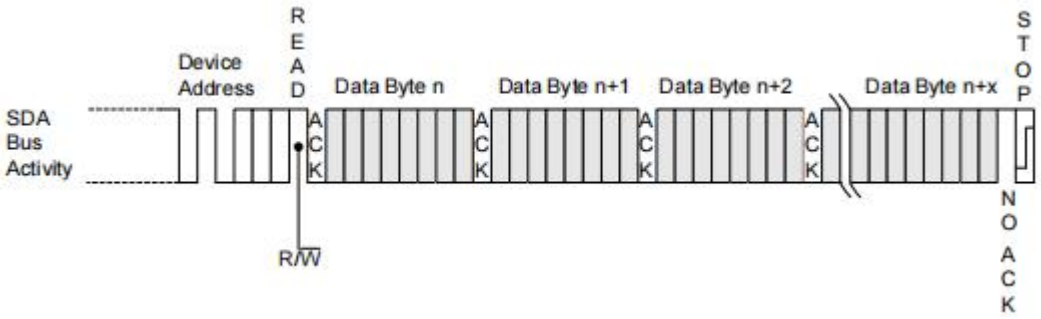


Figure 10.Sequential Read

5.11 Timing Diagrams

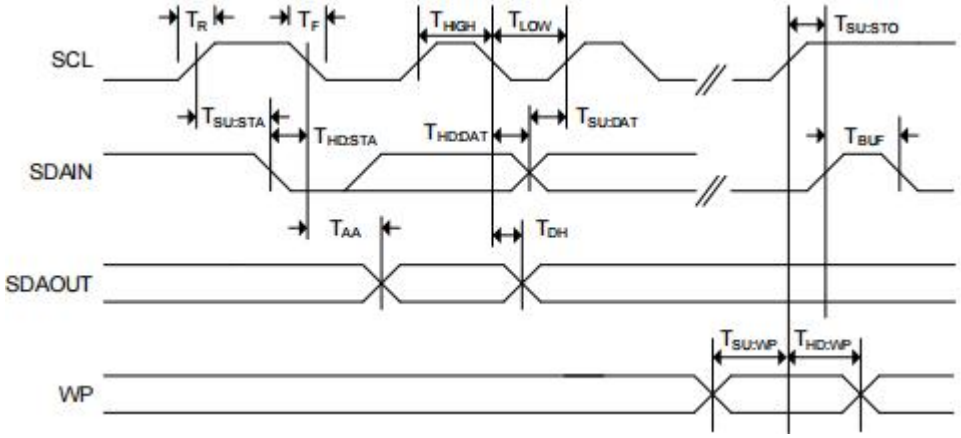


Figure 11. Bus Timing

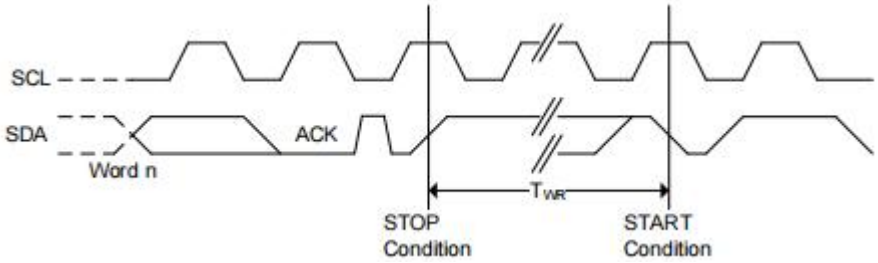


Figure 12. Write Cycle Timing

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	-0.5 to 6.5	V
V_P	Voltage on Any Pin	-0.5 to 6.5	V
T_{STG}	Storage Temperature	-65 to +150	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
I_{OUT}	Output Current	5	mA

Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

6.2 Operating Range

Range	Ambient Temperature (TA)	VCC
Industrial	–40°C to +85°C	1.7V to 5.5V

6.3 Capacitance

Symbol	Parameter[1, 2]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input / Output Capacitance	$V_{I/O}$ = 0V	8	pF

Notes: [1] Tested initially and after any design or process changes that may affect these parameters and not 100% tested.

[2] Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V.

6.4 DC Electrical Characteristic

Industrial: T_A = –40°C to +85°C, V_{CC} = 1.7V ~ 5.5V

Symbol	Parameter [1]	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		1.7		5.5	V
V_{IH}	Input High Voltage(WP and A0, A1, A2)		0.7*V_{CC}		V_{CC}+0.5	V
	Input High Voltage(SCL and SDA)		0.7*V_{CC}		V_{CC}+0.5	V
V_{IL}	Input Low Voltage		-0.5		0.3* V_{CC}	V
I_{LI}	Input Leakage Current	Vcc=5V, V_{IN} = $V_{CC\ max}$	—		2	μA
I_{LO}	Output Leakage Current	Vcc=5V	—		2	μA
V_{OL1}	Output Low Voltage	Vcc=1.7V,I_{OL} = 0.15 mA	—		0.2	V
V_{OL2}	Output Low Voltage	Vcc=2.5V,I_{OL} = 2.1 mA	—		0.4	V
I_{SB1}	Standby Current	Vcc=1.7V,V_{IN} = V_{CC} or GND	—	0.2	1	μA
I_{SB2}	Standby Current	Vcc=2.5V,V_{IN} = V_{CC} or GND	—	0.3	1	μA
I_{SB3}	Standby Current	Vcc=5.5V,V_{IN} = V_{CC} or GND	—	0.5	1	μA
I_{CC1}	Read Current	Vcc=1.7V,Read at 400 KHz	—		0.3	mA
		Vcc=2.5V,Read at 1 MHz	—		0.3	mA
		Vcc=5.5V,Read at 1 MHz	—		0.5	mA
I_{CC2}	Write Current	Vcc=1.7V,Write at 400 KHz	—		0.4	mA
		Vcc=2.5V,Write at 1 MHz	—		0.6	mA
		Vcc=5.5V,Write at 1 MHz	—		0.8	mA

Note: The parameters are characterized but not 100% tested.

6.5 AC Electrical Characteristic

Industrial: T_A = –40°C to +85°C, Supply voltage = 1.7V to 5.5V

Symbol	Parameter [1] [2]	1.7V≤V_{CC}≤5.5V Slow Mode		1.7V≤VCC≤5.5V Fast Mode		Unit
		Min.	Max.	Min.	Max.	
F_{SCL}	SCK Clock Frequency		400		1000	KHz
T_{LOW}	Clock Low Period	1200	—	400	—	ns
T_{HIGH}	Clock High Period	600	—	400	—	ns
T_R	Rise Time (SCL and SDA)	—	300	—	300	ns
T_F	Fall Time (SCL and SDA)	—	300	—	100	ns
$T_{SU:STA}$	Start Condition Setup Time	500	—	200	—	ns
$T_{SU:STO}$	Stop Condition Setup Time	500	—	200	—	ns
$T_{HD:STA}$	Start Condition Hold Time	500	—	200	—	ns
$T_{SU:DAT}$	Data In Setup Time	100	—	40	—	ns
$T_{HD:DAT}$	Data In Hold Time	0	—	0	—	ns
T_{AA}	Clock to Output Access time (SCL Low to SDA Data Out Valid)	100	900	50	400	ns
T_{DH}	Data Out Hold Time (SCL Low to SDA Data Out Change)	100	—	50	—	ns
T_{WR}	Write Cycle Time	—	5	—	5	ms
T_{BUF}	Bus Free Time Before New Transmission	1000	—	400	—	ns
$T_{SU:WP}$	WP pin Setup Time	1000	—	400		ns
$T_{HD:WP}$	WP pin Hold Time	1200	—	1200	—	ns
T	Noise Suppression Time	—	100	—	50	ns
Endr	Endurance (5.5V, 25C, byte mode & page mode)	1 million				cycles

Notes:

[1] The parameters are characterized but not 100% tested.

[2] AC measurement conditions:

R_L (connects to V_{CC}): 1.3 kΩ (2.5V, 5V), 10 kΩ (1.7V)

C_L = 100 pF

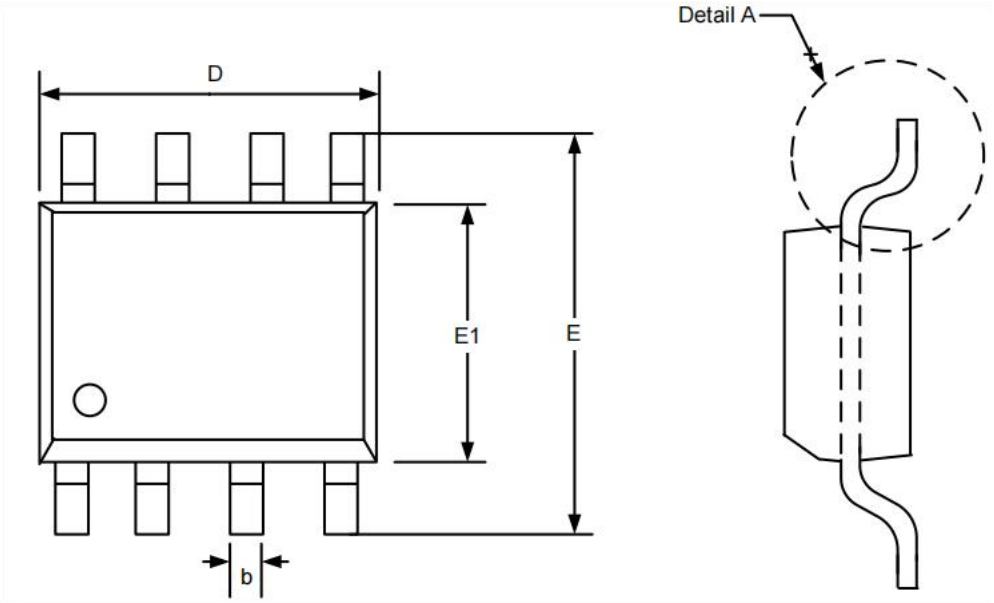
Input pulse voltages: 0.3*V_{CC} to 0.7*V_{CC}

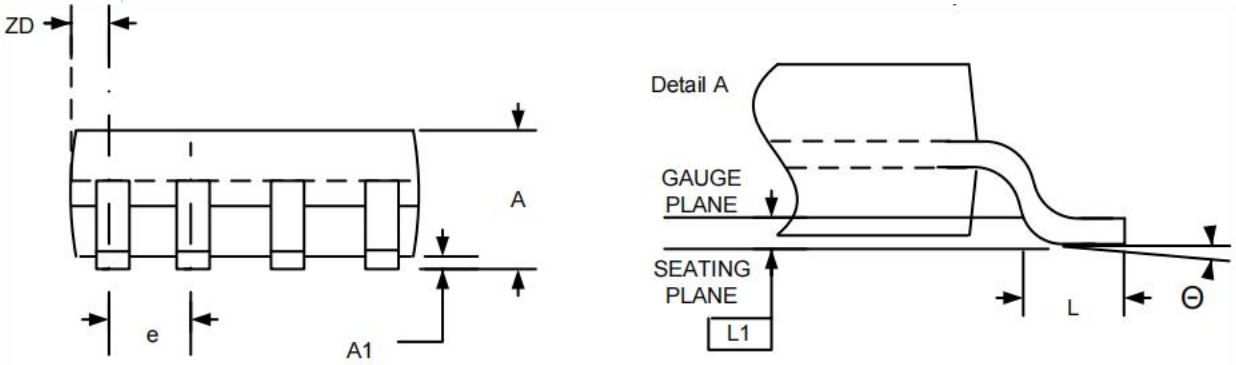
Input rise and fall times: ≤ 50 ns

Timing reference voltages: half V_{CC} level

7. Package Outline Dimensions(All dimensions in mm.)

(1) Package Type: SOP8



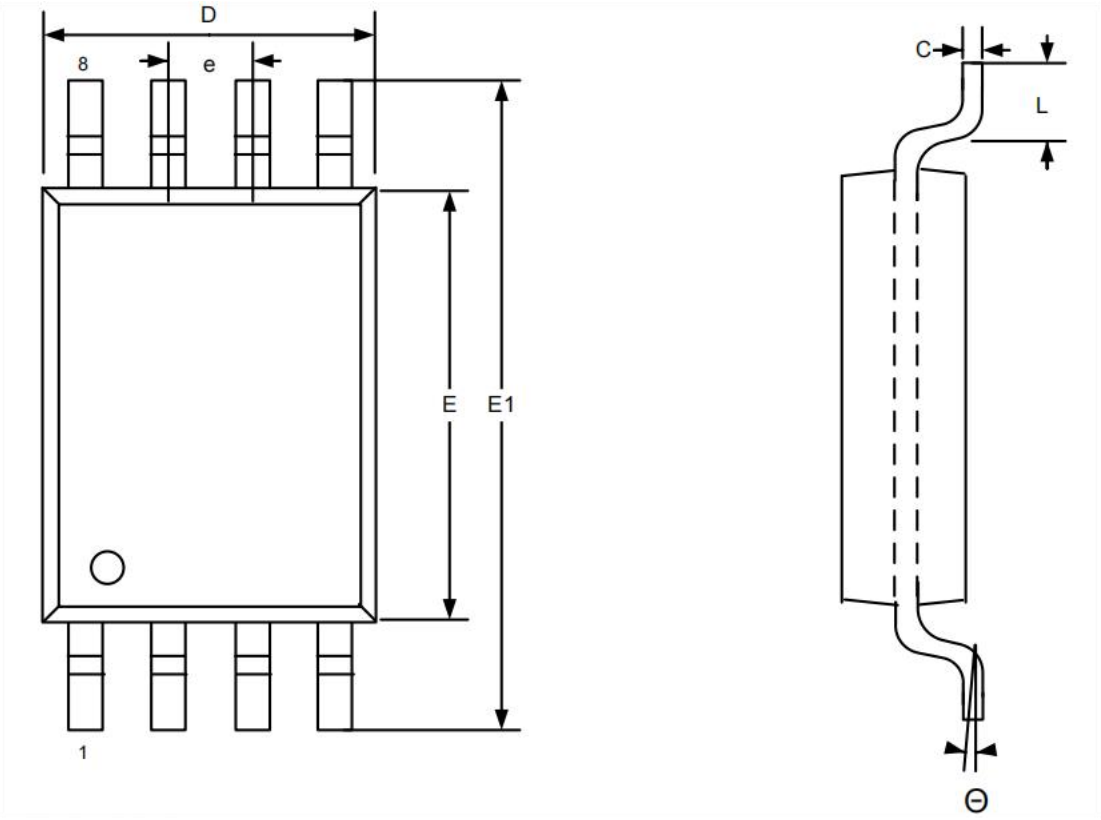


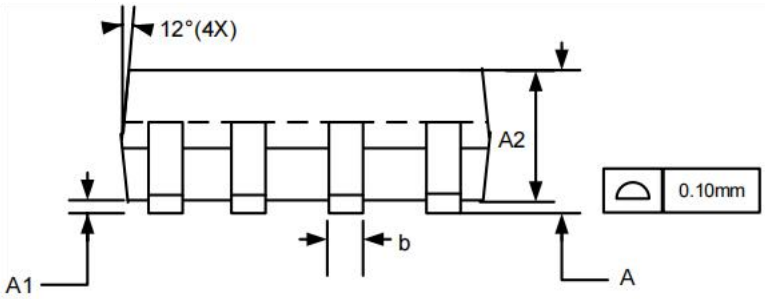
SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	--	1.75	0.053	--	0.069
A1	0.10	--	0.25	0.004	--	0.010
b	0.33	--	0.51	0.013	--	0.020
D	4.80	--	5.00	0.189	--	0.197
E	5.80	--	6.20	0.228	--	0.244
E1	3.80	--	4.00	0.150	--	0.157
e	1.27 BSC.			0.050 BSC.		
L	0.38	--	1.27	0.015		0.050
L1	0.25 BSC.			0.010 BSC.		
ZD	0.545 REF.			0.021 REF.		
Θ	0	--	8°	0	--	8°

Note:

1. Controlling Dimension:MM
2. Dimension D and E1 do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion.
4. Refer to Jedec standard MS-012
5. Drawing is not to scale

(2) Package Type: TSSOP8

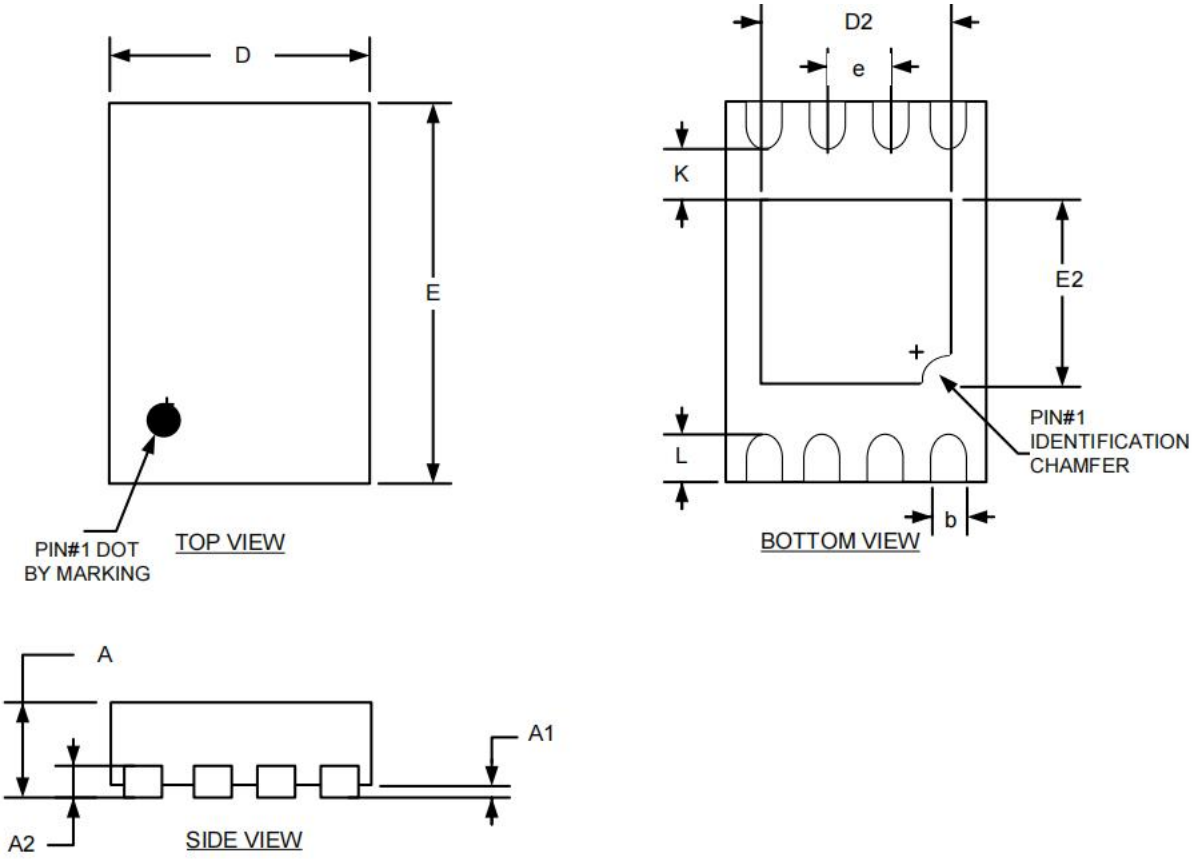




Note:
1. Controlling Dimension:MM
2. Dimension D and E do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion
4. Refer to Jedec standard MO-153 AA
5. Drawing is not to scale
6. Package may have exposed tie bar.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	--	--	1.20	--	--	0.047
A1	0.05	--	0.15	0.002	--	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	--	0.30	0.007	--	0.012
c	0.09	--	0.20	0.004	--	0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.30	4.40	4.50	0.169	0.173	0.177
E1	6.20	6.40	6.60	0.244	0.252	0.230
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
Θ	0	--	8°	0	--	8°

(3) Package Type: UDFN8

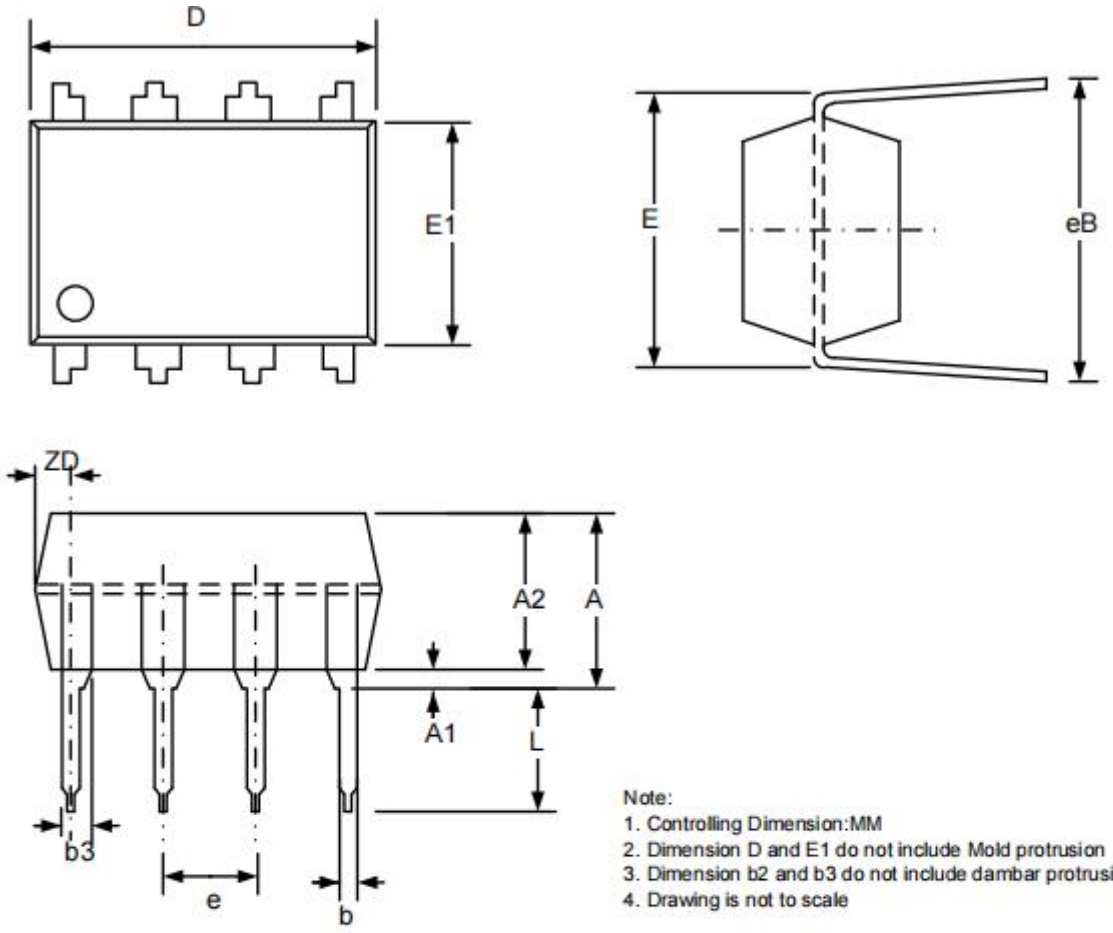


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	--	0.05	0.000	--	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
A2	0.152 REF			0.006 REF		
D	2.00 BSC			0.079 BSC		
D2	1.25	1.40	1.50	0.049	0.055	0.059
E	3.00 BSC			0.118 BSC		
E2	1.15	1.30	1.40	0.045	0.051	0.055
e	0.50 BSC.			0.020 BSC.		
K	0.40	--	--	0.016	--	--
L	0.20	0.30	0.40	0.008	0.012	0.016

Note:

1. Controlling Dimension:MM
2. Drawing is not to scale

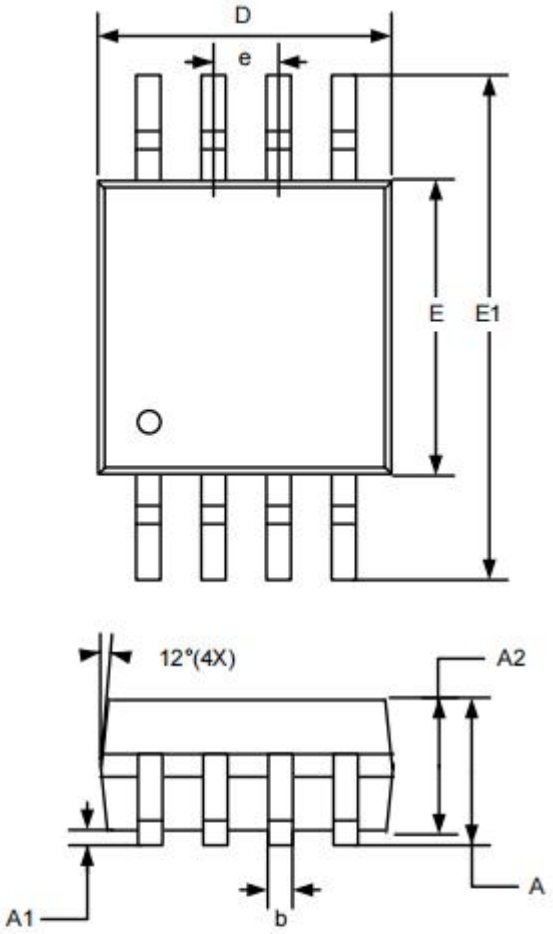
(4) Package Type: PDIP8



Note:
1. Controlling Dimension:MM
2. Dimension D and E1 do not include Mold protrusion
3. Dimension b2 and b3 do not include dambar protrusion/instrusion
4. Drawing is not to scale

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	3.60	–	4.20	0.142	–	0.165
A1	0.38	–	0.75	0.015	–	0.030
A2	3.25	–	3.45	0.128	–	0.136
b	0.36	–	0.56	0.014	–	0.022
b2	1.40	–	1.65	0.055	–	0.065
b3	0.81	–	1.17	0.032	–	0.046
D	9.01	–	9.53	0.355	–	0.375
E	7.49	–	8.26	0.295	–	0.325
E1	6.20	–	6.60	0.244	–	0.260
e	2.54 BSC.			0.100 BSC.		
eB	8.12	–	9.65	0.320	–	0.380
L	3.18	–	3.80	0.125	–	0.150
ZD	0.825 REF.			0.032 REF.		

(5) Package Type: MSOP8



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	--	--	1.10	--	--	0.043
A1	0.05	--	0.15	0.002	--	0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.25	--	0.40	0.010	--	0.016
C	0.13	--	0.23	0.005	--	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	4.90 BSC			0.193 BSC		
e	0.65 BSC			0.026 BSC		
L	--	--	0.55	--	--	0.022
Θ	0	--	7°	0	--	7°

Note:
1. Controlling Dimension:MM
2. Dimension D and E do not include Mold protrusion
3. Refer to Jedec standard MO187
4. Drawing is not to scale

8. Order information

Mode	Package	Ordering Number	Packing Option
FEP24C256	SOP8	FEP24C256YSOP8G/TR	Tape and Reel,2500
	TSSOP8	FEP24C256YTSSOP8G/TR	Tape and Reel,3000
	UDFN8	FEP24C256YUDFN8G/TR	Tape and Reel,4000
	MSOP8	FEP24C256YMSOP8G/TR	Tape and Reel,4000
	PDIP8	FEP24C256YPDIP8G/TR	Tape and Reel,2500

9. Important Notice And Disclaimer

- We reserves the right to change the instruction manual without prior notice.
- Any semiconductor product has a certain possibility of failure or malfunction under specific conditions. The buyer is responsible for complying with safety standards and taking safety measures when using our products for system design and overall manufacturing to avoid potential failure risks that may cause personal injury or property damage.
- The improvement of product quality is endless, our company will be dedicated to provide customers with better products.