

Three-Channel Differential 4:1 Super Speed & USB 2.0 Mux/DeMux

1.Descriptions

The FSW6820 is a high-speed bidirectional passive switch in mux or demux configurations . It suited for USB Type-C™ application supporting switch between four differential signals such as "USB super speed + USB high speed". Based on control pin SEL1 & SEL2, the device provides switching on differential channels between Port A or Port B or Port C to Port COM. The FSW6820 is a generic analog differ-ential passive switch that can work for any high-speed interface applications requiring a common mode voltage range of 0 to 2 V and differential signaling with differential amplitude up to 1800 mVpp. It employs adaptive tracking that ensures the channel remains unchanged for the entire common mode voltage range. Excellent dynamic characteristics of the device allow high-speed switching with minimum attenuation to the signal eye diagram with very little added jitter. It consumes <2mW of power when operational and has a shutdown mode exercisable by EN Pin resulting <20uW.

2.Features

- Three-Differential Channel 4:1 Mux/DeMux
- USB 3.1 Super Speed Switch
- USB 3.1 High Bandwidth: 5GHz @-3dB BW
- USB 2.0 Bandwidth:1GHz
- Supports both AC coupled and DC coupled signals
- Isolation: -42.88dB @ 5Ghz
- Crosstalk: -25.67dB @ 5Ghz
- ESD Tolerance: 2kV HBM
- Low bit-to-bit skew, Bidirectional

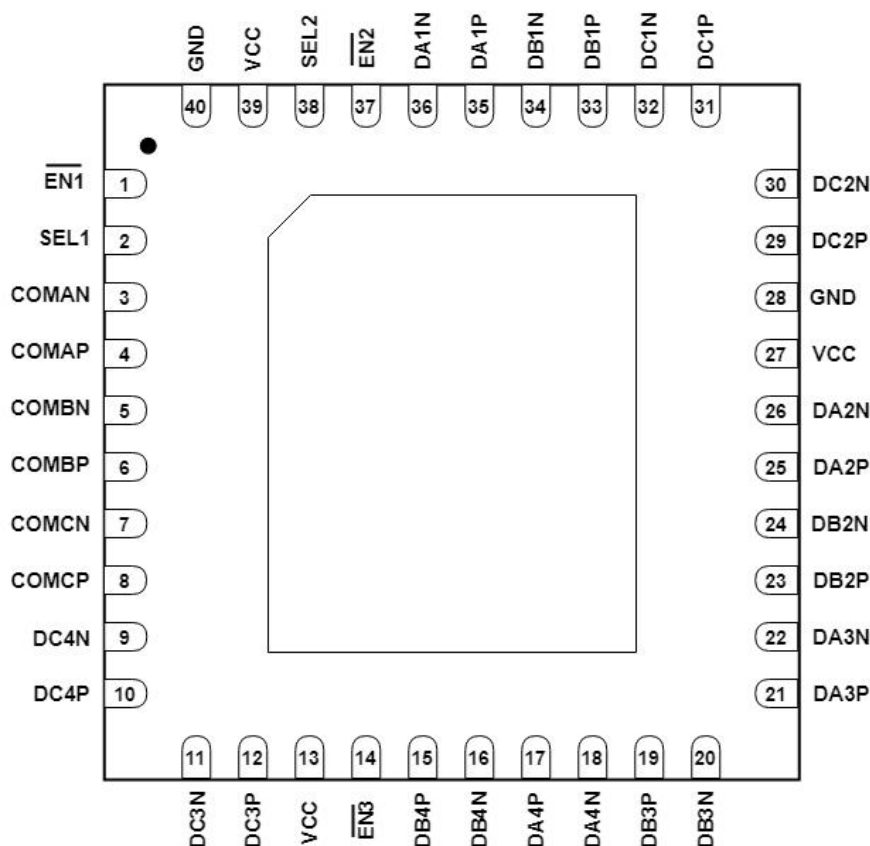
3.Applications

- USB Type-C Ecosystem
- Desktop and Notebook PCs
- Server/Storage Area Networks
- PCI Express Backplanes
- Shared I/O Ports
- FPD LinkII and FPD LinkIII Switching

4.Order information

Mode	Package	Specified Temperature range	Ordering Number	Packing Option
FSW6820	QFN5x5-40L	-40℃ to +85℃	FSW6820YQFN40G/TR	Tape and Reel,5000

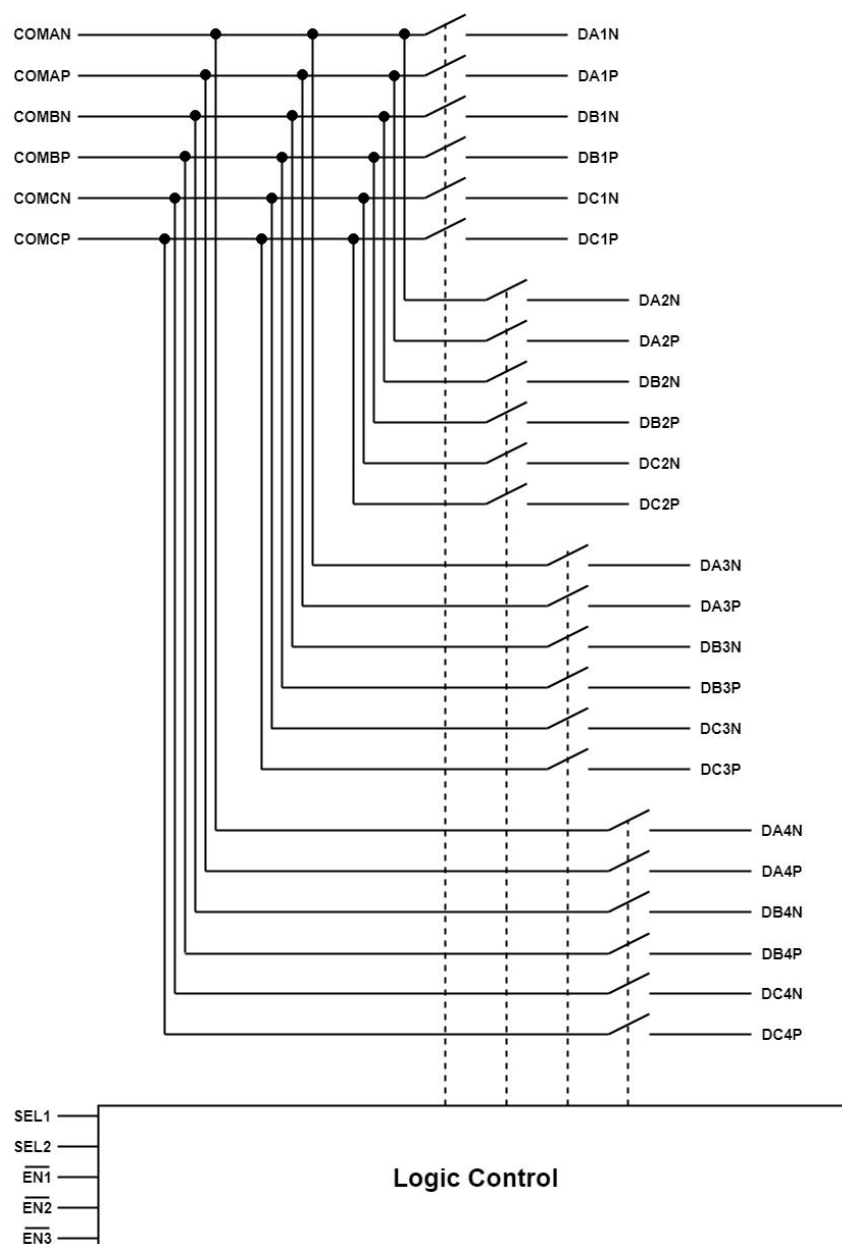
5.Pin Configuration



Pin#	Pin Name	Signal Type	Description
1	EN1	I	Enable Pin,Active Low
2	SEL1	I	Select Pin, See Truth Table
3	COMAN	I/O	Negative differential signal 1 for USB 3.1 port COM
4	COMAP	I/O	Positive differential signal 1 for USB 3.1 port COM
5	COMBN	I/O	Negative differential signal 2 for USB 3.1 port COM
6	COMBP	I/O	Positive differential signal 2 for USB 3.1 port COM
7	COMCN	I/O	Negative differential signal 3 for USB 2.0 port COM
8	COMCP	I/O	Positive differential signal 3 for USB 2.0 port COM
9	DC4N	I/O	Negative differential signal 4 for USB 2.0 port C
10	DC4P	I/O	Positive differential signal 4 for USB 2.0 port C
11	DC3N	I/O	Negative differential signal 3 for USB 2.0 port C
12	DC3P	I/O	Positive differential signal 3 for USB 2.0 port C
13	VCC	Power	Positive Supply Voltage
14	EN3	I	Enable Pin,Active Low
15	DB4P	I/O	Positive differential signal 4 for USB 3.1 port B

16	DB4N	I/O	Negative differential signal 4 for USB 3.1 port B
17	DA4P	I/O	Positive differential signal 4 for USB 3.1 port A
18	DA4N	I/O	Negative differential signal 4 for USB 3.1 port A
19	DB3P	I/O	Positive differential signal 3 for USB 3.1 port B
20	DB3N	I/O	Negative differential signal 3 for USB 3.1 port B
21	DA3P	I/O	Positive differential signal 3 for USB 3.1 port A
22	DA3N	I/O	Negative differential signal 3 for USB 3.1 port A
23	DB2P	I/O	Positive differential signal 2 for USB 3.1 port B
24	DB2N	I/O	Negative differential signal 2 for USB 3.1 port B
25	DA2P	I/O	Positive differential signal 2 for USB 3.1 port A
26	DA2N	I/O	Negative differential signal 2 for USB 3.1 port A
27	VCC	Power	Positive Supply Voltage
28	GND	Ground	Power Ground
29	DC2P	I/O	Positive differential signal 2 for USB 2.0 port C
30	DC2N	I/O	Negative differential signal 2 for USB 2.0 port C
31	DC1P	I/O	Positive differential signal 1 for USB 2.0 port C
32	DC1N	I/O	Negative differential signal 1 for USB 2.0 port C
33	DB1P	I/O	Positive differential signal 1 for USB 3.1 port B
34	DB1N	I/O	Negative differential signal 1 for USB 3.1 port B
35	DA1P	I/O	Positive differential signal 1 for USB 3.1 port A
36	DA1N	I/O	Negative differential signal 1 for USB 3.1 port A
37	$\overline{\text{EN2}}$	I	Enable Pin, Active Low
38	SEL2	I	Select Pin, See Truth Table
39	VCC	Power	Positive Supply Voltage
40	GND	Ground	Power Ground

6. Block Diagram



7.Truth Table

$\overline{\text{EN1}} \& \overline{\text{EN2}} \& \overline{\text{EN3}}$	SEL1	SEL2	Channel
High	X	X	X
Low	Low	Low	1
		High	2
	High	High	3
		Low	4

8.Absolute Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Parameter	Range
Storage Temperature	-65℃ to +150℃
Junction Temperature	125℃
Supply Voltage to Ground Potential	-0.5V to +5.5V
Supe Speed Data Channel TX / RX	-0.5V to 3.8V
DC Input Voltage	-0.5V to VCC
DC Output Current	50mA
Power Dissipation	300mW

Notes:

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

9. Electrical Characteristics

(T_A=25°C, V_{CC}=3V, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply						
VCC Quiescent Current	I _Q	SEL=0 or VCC, EN1 & EN2 & EN3 =0			100	uA
Power-down Current	I _{PO}	SEL=0 or VCC, EN1 & EN2 & EN3 =VCC			3	uA
DC Characteristics						
Input logic high	V _{IH}	VCC=1.8~4.5V	1.6			V
Input logic low	V _{IL}	VCC=1.8~4.5V			0.4	V
EN Internal pull-up resistor	R _{UP}			2		MΩ
SEL Internal pull-down resistor	R _{DN}			2		MΩ
On-Resistance for TX/RX	R _{ON_HS}	V _{IS} = 1.5V I _{ON} =10mA		13.4		Ω
R _{ON} Matching Between Channels	R _{MATCH}	V _{IS} = 0 to 1.2V I _{ON} =10mA		0.1		Ω
AC Characteristics						
Enable Time EN to Output	t _{EN}	R _L =50Ω C _L =0pF V _{IS} = 0.6V		80	150	uS
Disable Time EN to Output	t _{DIS}	R _L =50Ω C _L =0pF V _{IS} = 0.6V		40	250	nS
Turn-On Time SEL to Output	t _{ON}	R _L =50Ω C _L =0pF V _{IS} = 0.6V		400	1200	nS
Turn-Off Time SEL to Output	t _{OFF}	R _L =50Ω C _L =0pF V _{IS} = 0.6V		130	800	nS
Break-Before-Make Time	t _{BBM}	R _L =50Ω C _L =0pF V _{IS} = 0.6V		250	800	nS
Propagation Delay	t _{PD}	R _L =50Ω C _L =0pF V _{IS} = 0.6V		0.25		nS
Off Isolation	Off	R _L = 50Ω f = 5GHz V _{IS} = 0.2V _{PP} , See Fig.2		-42.88		dB
Crosstalk	X _{TALK}	R _L = 50Ω f = 5GHz V _{IS} = 0.2V _{PP} , See Fig.1		-25.67		dB
-3dB Bandwidth	BW _{-3dB}	R _L =50Ω C _L =0pF Signal 0dBm		5		GHz
Insertion Loss	IL	f=5GHz		-2.97		dB
Return Loss	RL	f=5GHz		-10.07		dB
Capacitance						
Switch On Capacitance	C _{ON}	V _{Bias} = 0.2V, f = 1.5GHz		1.5		pF
Switch Off Capacitance	C _{OFF}	V _{Bias} = 0.2V, f = 1.5GHz		1.0		pF

Notes:

- (1) Flatness is defined as the difference between maximum and minimum value of ON-resistance at the specified analog signal voltage points.
- (2) R_{ON} matching between channels is calculated by subtracting the channel with the lowest max Ron value from the channel with the highest max Ron value.
- (3) Crosstalk is inversely proportional to source impedance

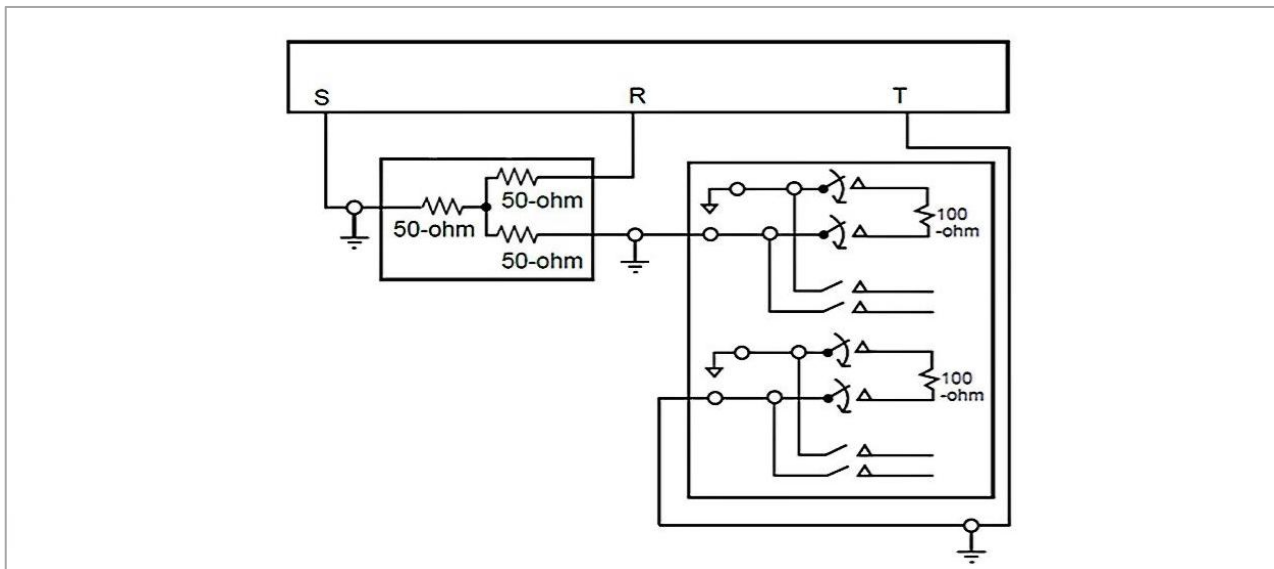


Fig.1 Crosstalk Setup

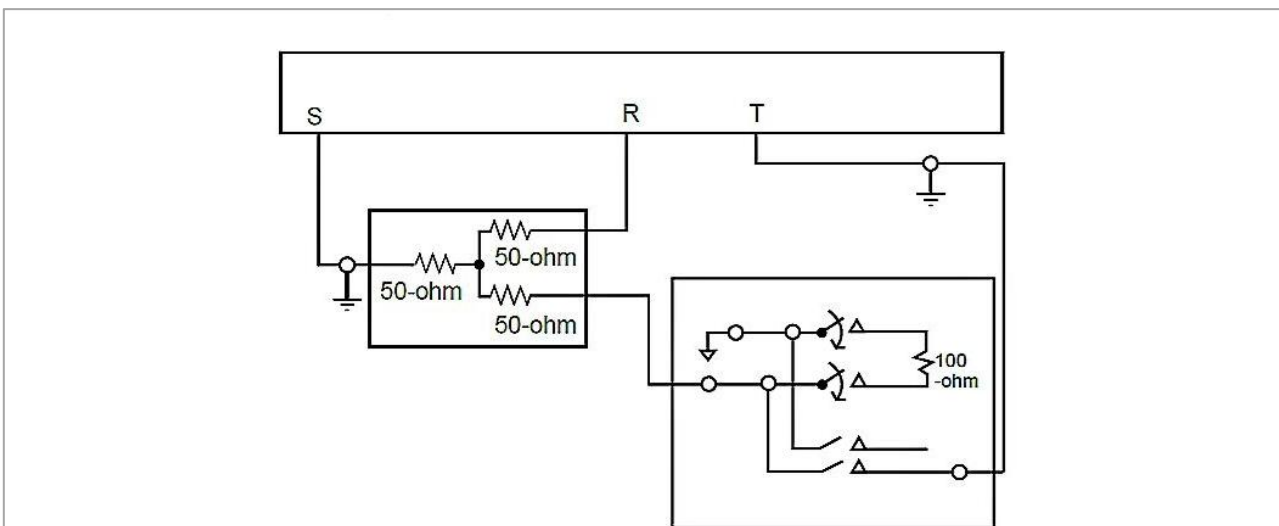


Fig.2 OFF-isolation

10.Application Information

Many interfaces require AC coupling between the transmitter and receiver. The 0402 capacitors are the preferred option to provide AC coupling, and the 0603 size capacitors also work. The 0805 size capacitors and C-packs should be avoided. When placing AC coupling capacitors symmetric placement is best. A capacitor value of 0.1 μF is best and the value should be match for the $\pm$ signal pair. The placement should be along the TX pairs on the system board, which are usually routed on the top layer of the board.

There are several placement options for the AC coupling capacitors. Because the switch requires a bias voltage, the capacitors must only be placed on one side of the switch. If they are placed on both sides of the switch, a biasing voltage should be provided. A few placement options are shown below. In Figure 1, the coupling capacitors are placed between the switch and endpoint. In this situation, the switch is biased by the system/host controller.

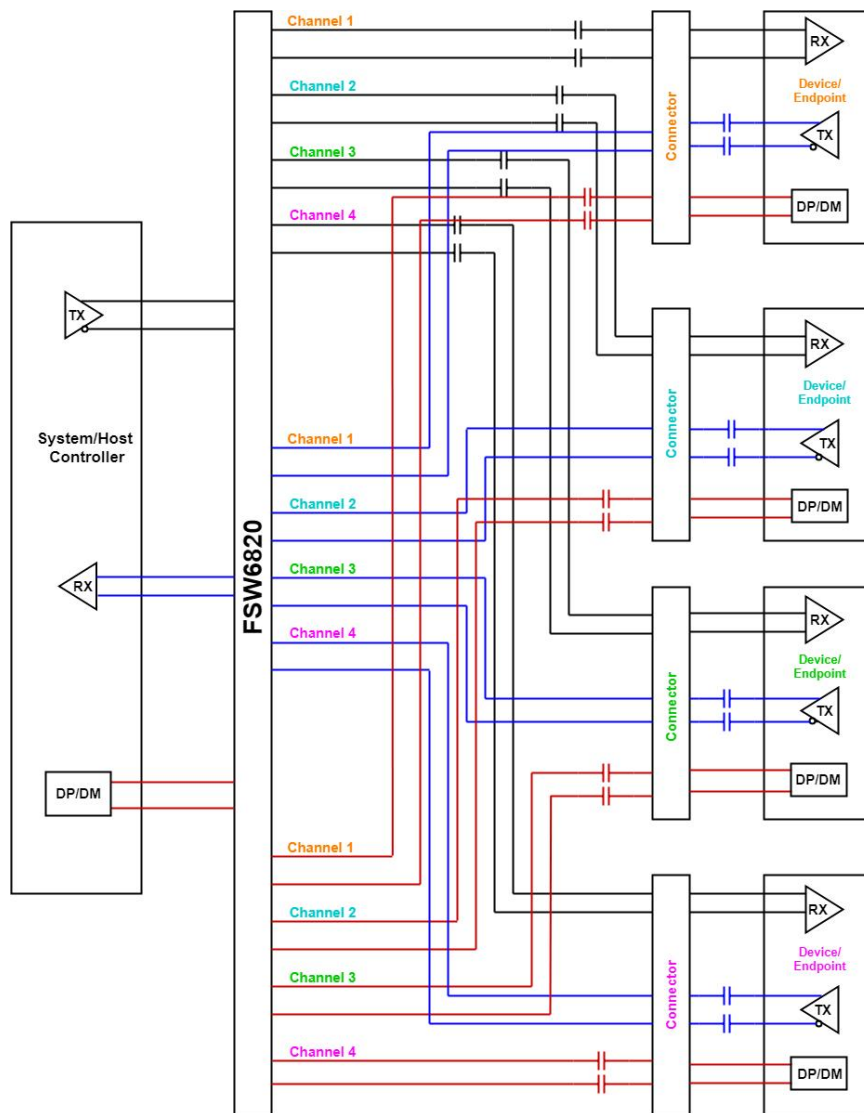


Figure 1. AC Coupling Capacitors Between Switch Tx and Endpoint Tx

In Figure 2, the coupling capacitors are placed on the host transmit pair and endpoint transmit pair. In this situation, the switch on the top is biased by the endpoint and the lower switch is biased by the host controller.

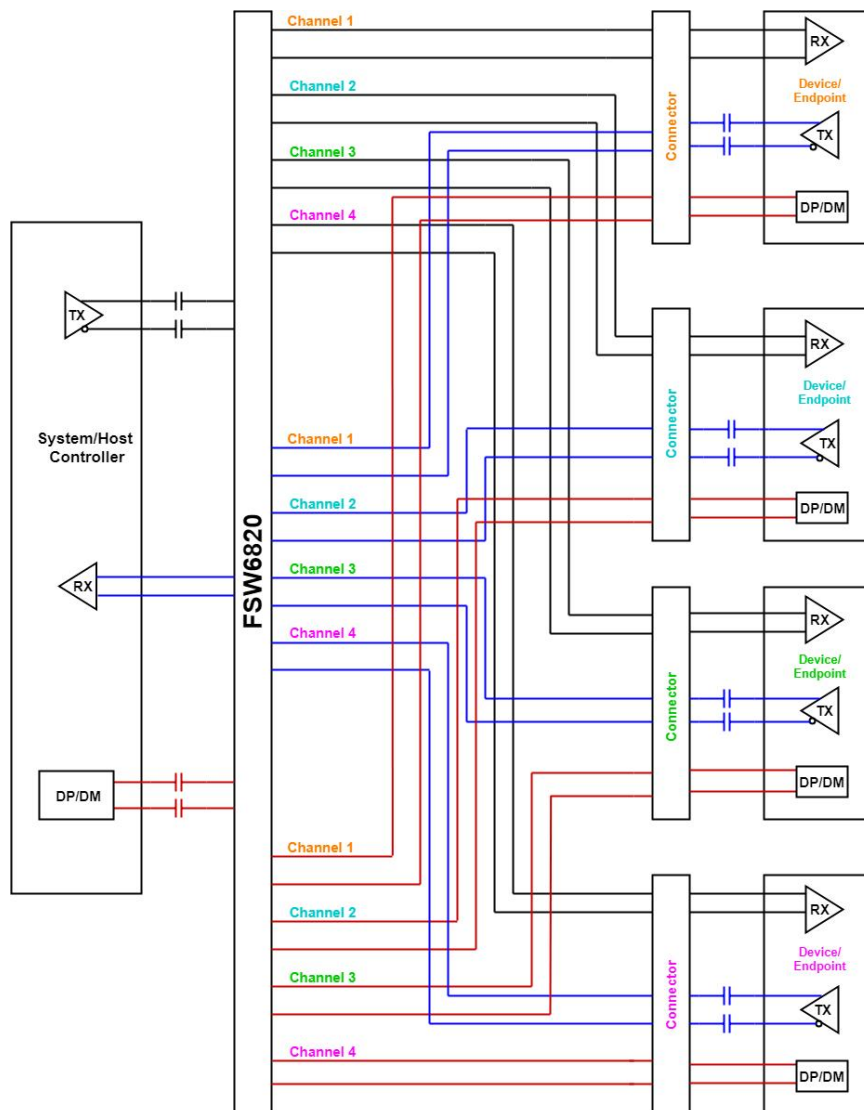


Figure 2. AC Coupling Capacitors on Host Tx and Endpoint Tx

If the common-mode voltage in the system is higher than 2V, the coupling capacitors are placed on both sides of the switch (shown in Figure 3). A biasing voltage of less than 2V is required in this case.

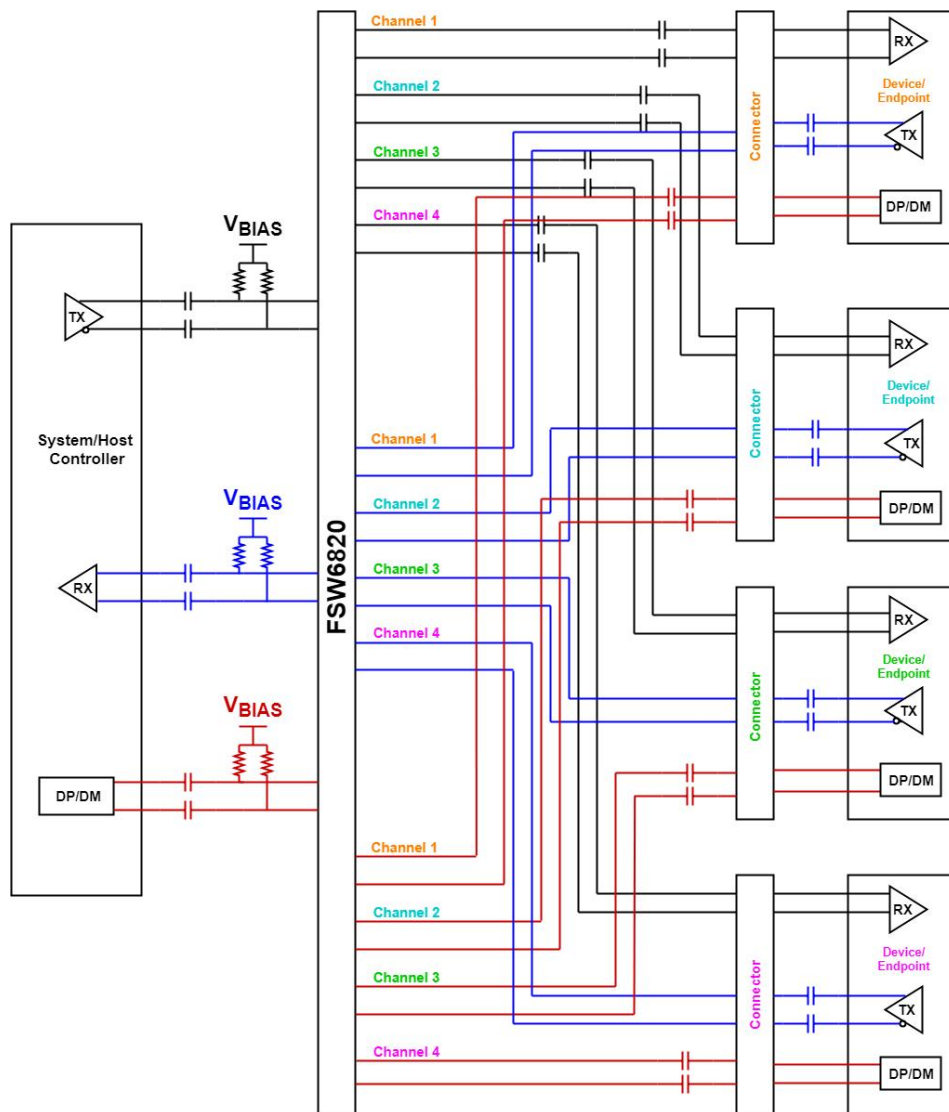
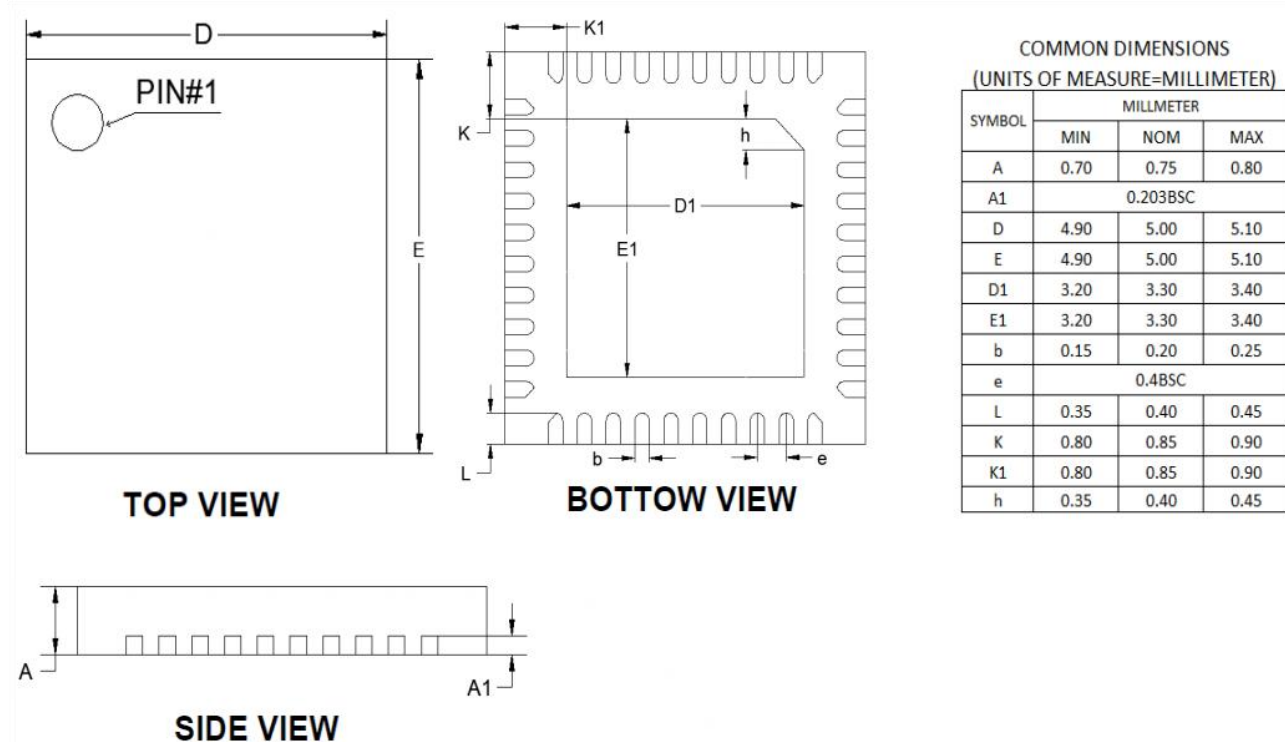


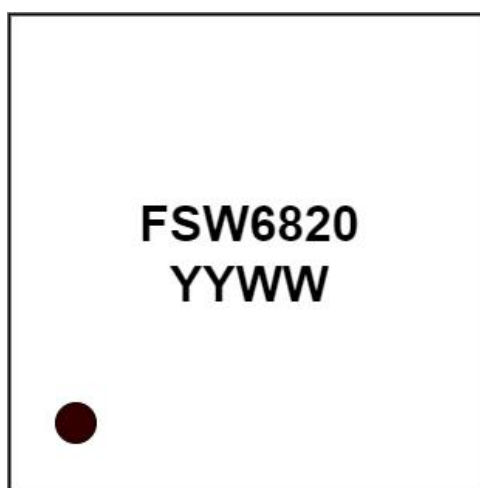
Figure 3. AC Coupling Capacitors on Both Sides of Switch

11.Package Outline Dimensions(All dimensions in mm.)

(1) Package Type: QFN5x5-40L



(2) Top Marking Information

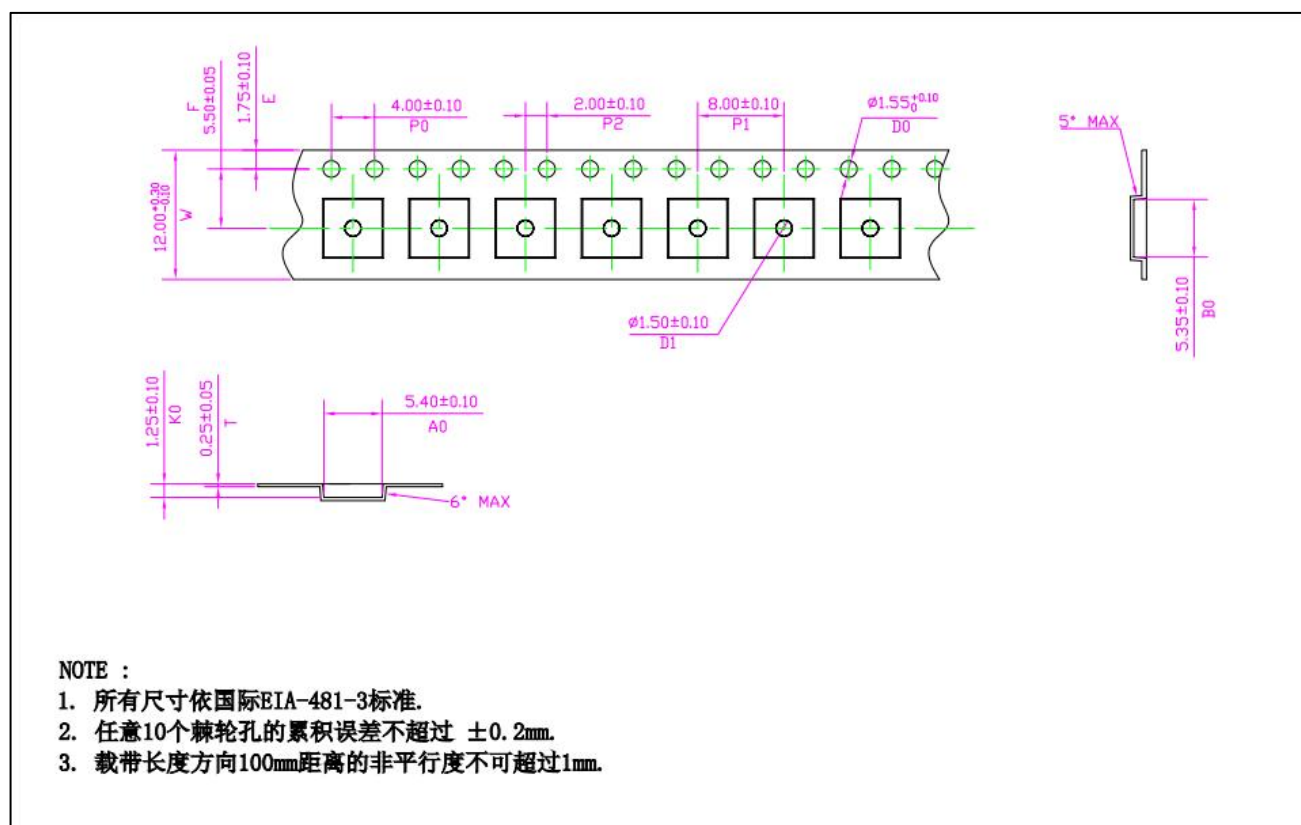
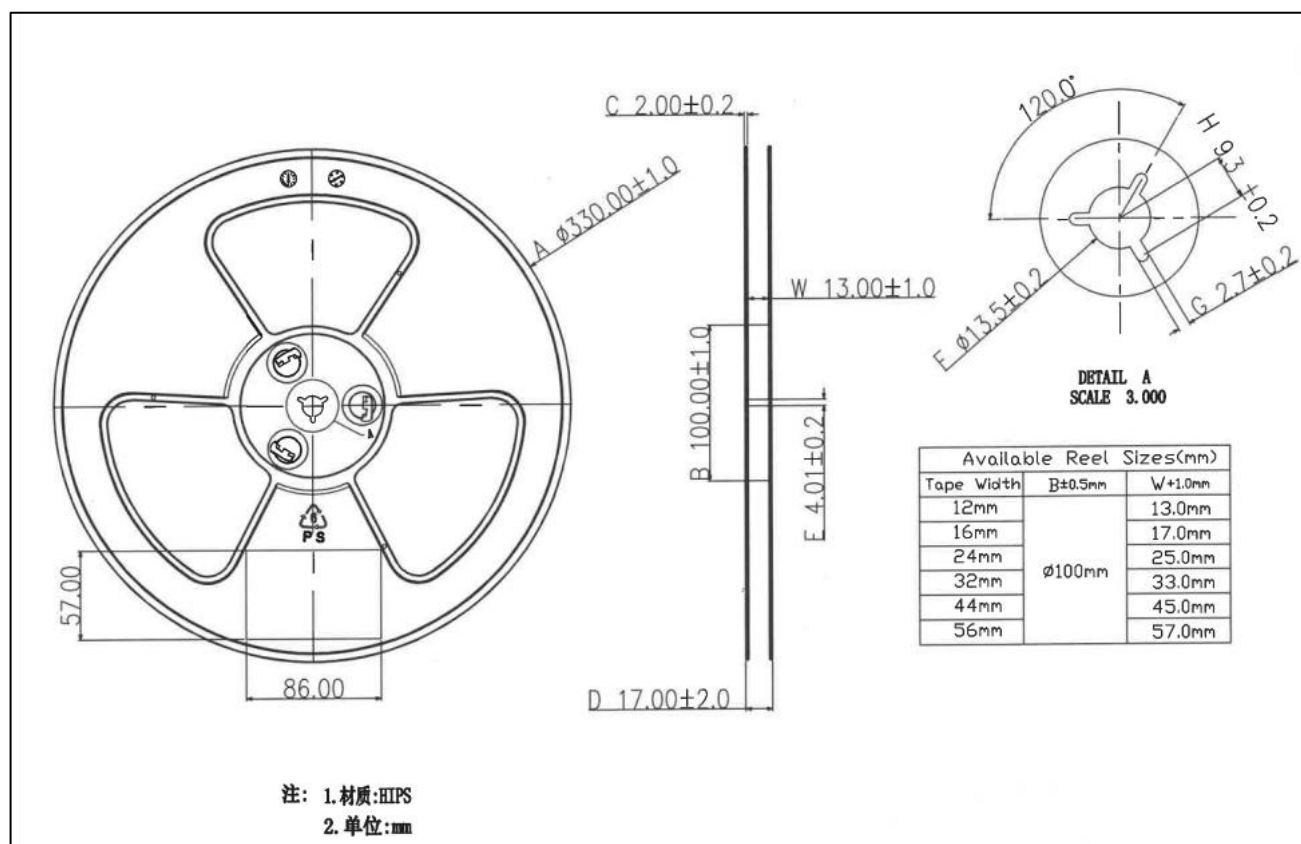


YY: Year (23=2023,24=2024...)

WW: Weekly (01-53)

FSW6820: mode

12. Tape And Reel Information



13.Important Notice And Disclaimer

- We reserves the right to change the instruction manual without prior notice.
- Any semiconductor product has a certain possibility of failure or malfunction under specific conditions. The buyer is responsible for complying with safety standards and taking safety measures when using our products for system design and overall manufacturing to avoid potential failure risks that may cause personal injury or property damage.
- The improvement of product quality is endless, our company will be dedicated to provide customers with better products.

14.Version Modification Record

Version Number	Revision
first edition	
V1.0	1.Update the test condition and “On-Resistance for TX/RX” of “Electrical Characteristics” on page 6
V2.0	1.Update the Electrical Characteristics on page 6 2.Update the Features on page 1.
V3.0	1.Update the Important Notice And Disclaimer on page 13.
V4.0	1.Update the Features on page 1. 2.Update the Electrical Characteristics on page 6
V4.1	1.Update the Top Making Information on page 11.