Five-Channel Differential 2:1 Super Speed & Two Normal Speed Signal Mux/DeMux

1.Descriptions

The FSW6862 is a high-speed and normal-speed bidirectional passive switch in mux or demux configurations.

The FSW6862 suited for suited for HDMI application supporting. Based on control pin SEL, the device provides switching on differential channels between Port A or Port B to Port COM. The FSW6862 is a generic analog differential passive switch that can work for any high-speed interface applications requiring a common mode voltage range of 0 to 2 V and differential signaling with differential amplitude up to 1800 mVpp. It employs adaptive tracking that ensures the channel remains unchanged for the entire common mode voltage range. Excellent dynamic characteristics of the device allow high-speed switching with mini-mum attenuation to the signal eye diagram with very little added jitter. It consumes <2mW of power when operational and has a shutdown mode exercisable by EN Pin resulting <20uW.

The FSW6862 normal speed signal is a single, bidirectional, single-pole/ double-throw (SPDT) CMOS analog switch.It target applications for audio switching.It features guaranteed on-resistance matching between switches and guaranteed on-resistance flatness over the signal range. This ensures excellent linearity and low distortion when switching audio signals.

2.Features

High Speed Channel :

- Five-Differertial Channel 2:1 Mux/DeMux
- HDMI2.0 Switch
- High Bandwidth: 7.5GHz @-3dB
- Supports both AC coupled and DC coupled
- signals
- Isolation: -39dB @ 5GHz
- Crosstalk: -41dB @ 5GHz
- ESD Tolerance: 2kV HBM
- Low bit-to-bit skew, Bidirectional
- Normal Speed Signal:
- High Bandwidth: 600MHz @-3dB
- High Off-Isolation: -100dB at 100KHz
- Low Channel to Channel Crosstalk: 97dB
- @100KHz

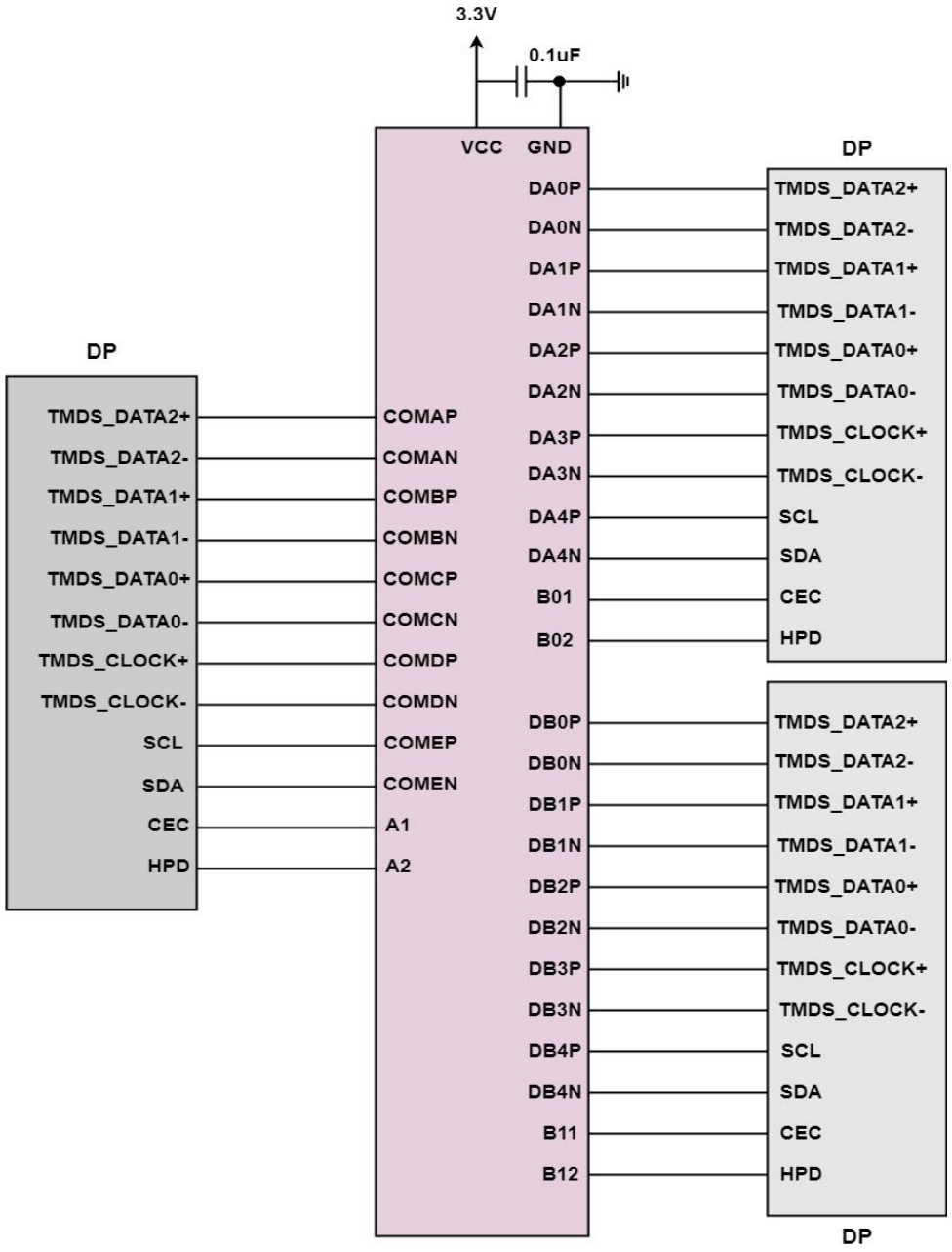
3.Applications

- HDMI2.0 With Support for 4k2k up to 60 Hz
- DVI1.0 Signal Switching
- DisplayPort 1.4 Signal Switching
- General Purpose TMDS Signal Switching
- General Purpose LVDS Signal Switching
- General Purpose High-Speed Signal Switching

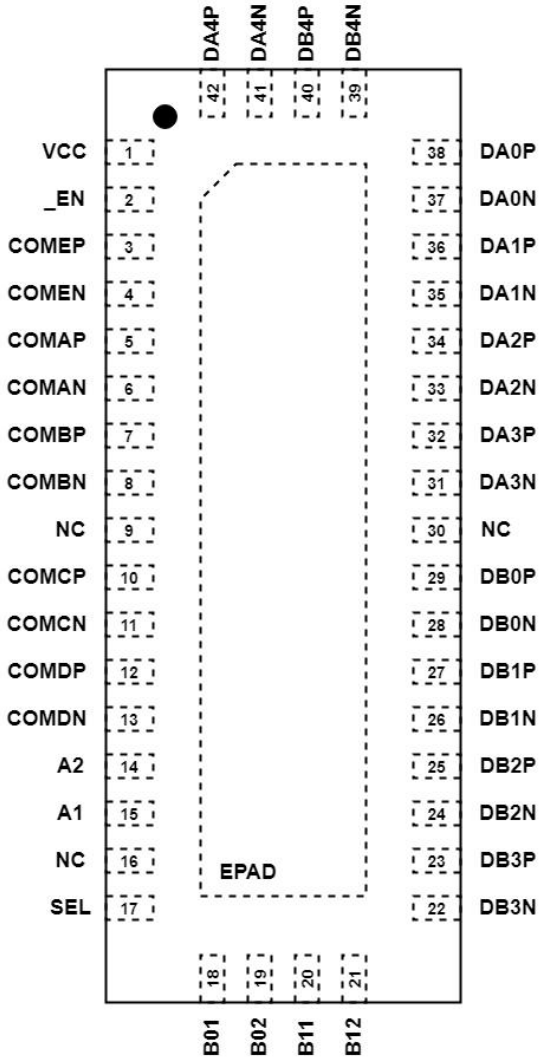
4.Order information

Mode	Package	Specified Temperature range	Ordering Number	Packing Option
FSW6862	LGA42-3.5x9.0	-40℃ to +85℃	FSW6862YLGA42G/TR	Tape and Reel,3000

5.Application Information



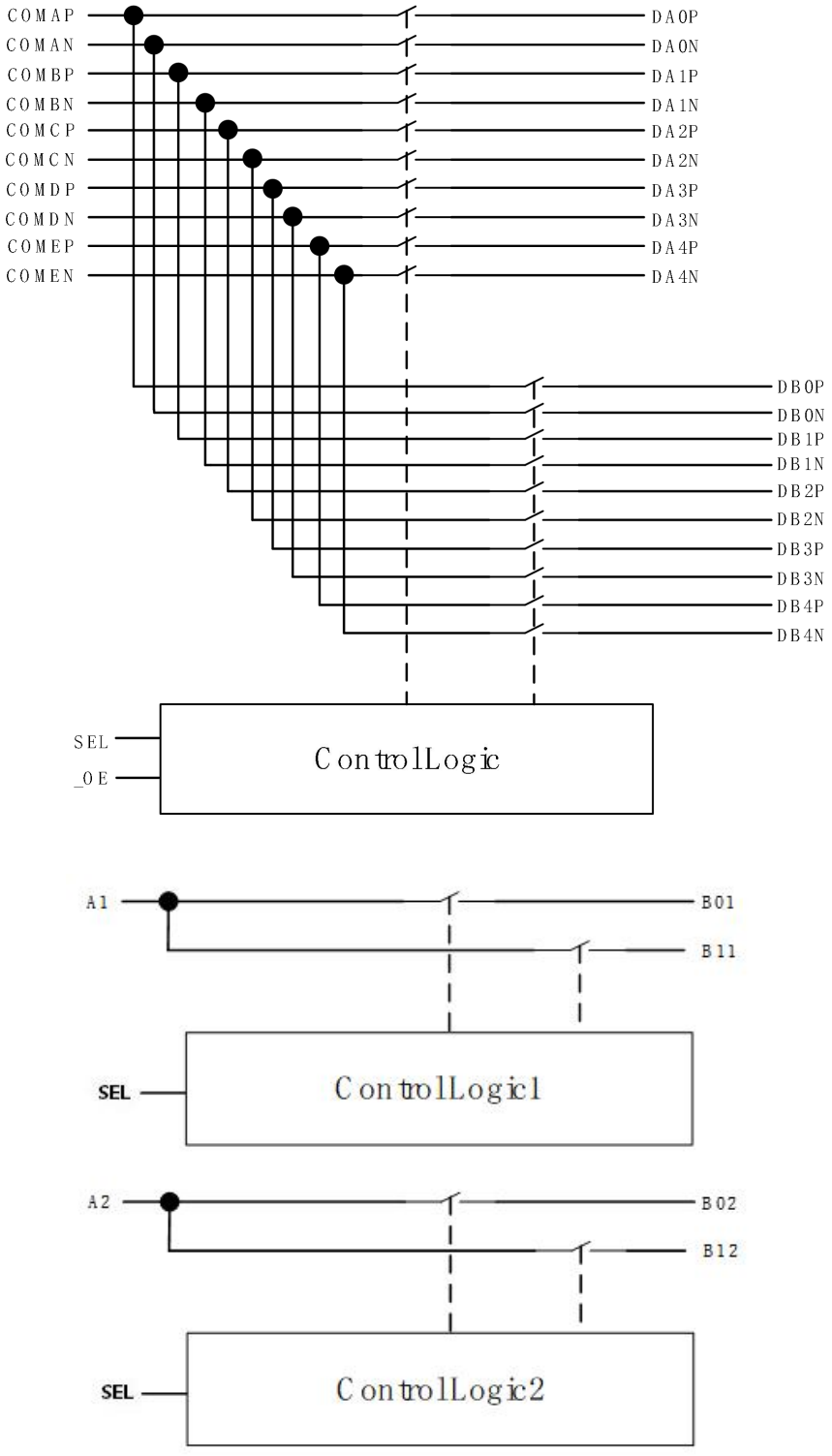
6.Pin Configuration



Pin#	Pin Name	Signal Type	Description
1	VCC	Power	Power Supply Voltage
2	_EN	I	Enable Pin, Active Low
3	COMEP	I/O	Positive differential signal 5 for port COM
4	COMEN	I/O	Negative differential signal 5 for port COM
5	COMAP	I/O	Positive differential signal 1 for port COM
6	COMAN	I/O	Positive differential signal 1 for port COM
7	COMBP	I/O	Positive differential signal 2 for port COM
8	COMBN	I/O	Negative differential signal 2 for port COM
9	NC	-	Not Connected
10	COMCP	I/O	Positive differential signal 3 for port COM
11	COMCN	I/O	Negative differential signal 3 for port COM
12	COMDP	I/O	Positive differential signal 4 for port COM
13	COMDN	I/O	Negative differential signal 4 for port COM

14	A2	I/O	Common Signal Port2
15	A1	I/O	Common Signal Port1
16	NC	-	Not Connected
17	SEL	I	Select Pin, See Truth Table. L:Port COM to Port A H:Port COM toPort B
18	B01	I/O	Analog/Digital Signal Port1 (Normally closed)
19	B02	I/O	Analog/Digital Signal Port2 (Normally closed)
20	B11	I/O	Analog/Digital Signal Port1 (Normally open)
21	B12	I/O	Analog/Digital Signal Port2 (Normally open)
22	DB3N	I/O	Negative differential signal 3 for port B
23	DB3P	I/O	Positive differential signal 3 for port B
24	DB2N	I/O	Negative differential signal 2 for port B
25	DB2P	I/O	Positive differential signal 2 for port B
26	DB1N	I/O	Negative differential signal 1 for port B
27	DB1P	I/O	Positive differential signal 1 for port B
28	DB0N	I/O	Negative differential signal 0 for port B
29	DB1P	I/O	Positive differential signal 0 for port B
30	NC	-	Not Connected
31	DA3N	I/O	Negative differential signal 3 for port A
32	DA3P	I/O	Positive differential signal 3 for port A
33	DA2N	I/O	Negative differential signal 2 for port A
34	DA2P	I/O	Positive differential signal 2 for port A
35	DA1N	I/O	Negative differential signal 1 for port A
36	DA1P	I/O	Positive differential signal 1 for port A
37	DA0N	I/O	Negative differential signal 0 for port A
38	DA0P	I/O	Positive differential signal 0 for port A
39	DB4N	I/O	Negative differential signal 4 for port B
40	DB4P	I/O	Positive differential signal 4 for port B
41	DA4N	I/O	Negative differential signal 4 for port A
42	DA4P	I/O	Positive differential signal 4 for port A
43	EPAD	Ground	Ground

7.Block Diagram



8.Truth Table

_OE	SEL	Channel
High	X	X
Low	Low	A
	High	B
_OE	SEL	Channel
High	X	X
Low	Low	B01
	High	B11
_OE	SEL	Channel
High	X	X
Low	Low	B02
	High	B12

9.Absolute Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Parameter	Range
Storage Temperature	-55℃ to +150℃
Junction Temperature	125℃
High Speed Channel	
Supply Voltage to Ground Potential	-0.5V to +5.5V
Super Speed Data Channel TX / RX	-0.5V to 3.8V
DC Input Voltage	-0.5V to 5.5V
DC Output Current	50mA
Power Dissipation	300mW
Normal Speed Channel	
Supply Voltage	-0.3~6.5V
Control Input Voltage	-0.3 ~ 6.5V
Continuous Current Through A1, B01, B11	±100mA
Continuous Current Through A2, B02, B12	±100mA
Peak Current Through A1, B01, B11 (pulsed at 1ms 50% duty cycle)	±200mA
Peak Current Through A1, B01, B11 (pulsed at 1ms 50% duty cycle)	±200mA
Thermal resistance	350°C/W

Notes:

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

10.Electrical Characteristics

(High speed channel,T_A=25°C, V_{CC}=3V, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply (High Speed Channel)						
VCC Quiescent Current	I_Q	SEL=0 or VCC, _EN=0			28	uA
Power-down Current	I_{PO}	SEL=0 or VCC, _EN=VCC			1	uA
DC Characteristics (High Speed Channel)						
Input logic high	V_{IH}	VCC=1.8~4.5V	1.6			V
Input logic low	V_{IL}	VCC=1.8~4.5V			0.4	V
$\overline{EN}$ Internal pull-up resistor	R_{UP}			2		MΩ
SEL Internal pull-down resistor	R_{DN}			2		MΩ
On-Resistance for TX/RX	R_{ON_HS}	V_{IS}= 1.5V I_{ON}=8mA		6.5		Ω
R_{ON} Matching Between Channels	R_{MATCH}	V_{IS}= 0 to 1.2V I_{ON}=8mA		0.1		Ω
AC Characteristics (High Speed Channel)						
Enable Time $\overline{EN}$ to Output	t_{EN}	R_L=50Ω C_L=0pF V_{IS}= 0.6V		80	150	uS
Disable Time $\overline{EN}$ to Output	t_{DIS}	R_L=50Ω C_L=0pF V_{IS}= 0.6V		40	250	nS
Turn-On Time SEL to Output	t_{ON}	R_L=50Ω C_L=0pF V_{IS}= 0.6V		400	1200	nS
Turn-Off Time SEL to Output	t_{OFF}	R_L=50Ω C_L=0pF V_{IS}= 0.6V		130	800	nS
Break-Before-Make Time	t_{BBM}	R_L=50Ω C_L=0pF V_{IS}= 0.6V		250	500	nS
Propagation Delay	t_{PD}	R_L=50Ω C_L=0pF V_{IS}= 0.6V		0.25		nS
Off Isolation	Off	R_L = 50Ω f = 5GHz V_{IS}= 0.2V_{PP}, See Fig.2		-39		dB
Crosstalk	X_{TALK}	R_L = 50Ω f = 5GHz V_{IS}= 0.2V_{PP}, See Fig.1		-41		dB
-3dB Bandwidth	BW_{-3dB}	R_L=50Ω C_L=0pF Signal 0dBm		7.5		GHz
Insertion Loss	IL	f=5GHz		-1.48		dB
Return Loss	RL	f=5GHz		-12.62		dB
Capacitance (High Speed Channel)						
Switch On Capacitance	C_{ON}	V_{Bias} = 0.2V, f = 1.5GHz		1.5		pF
Switch Off Capacitance	C_{OFF}	V_{Bias} = 0.2V, f = 1.5GHz		1.0		pF

(Normal Speed Channel,T_A=25°C, V_{CC}=3.3V, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max	Unit
DC Characteristics (Normal Speed Channel)						
Input logic high level	V_{IH}	VCC=3.3~5.5V	1.6			V
		VCC=1.5~3.3V	1.4			V
Input logic low level	V_{IL}	VCC=3.3~5.5V			0.6	V
		VCC=1.5~3.3V			0.4	V
Supply quiescent current	I_{CC}	I_A=0, V_{SEL} =0 or V_{SEL} =VCC			2.0	uA
Increase in I_{CC} per input	I_{CCT}	I_A=0, VCC=4.5V V_{SEL}>1.8 or V_{SEL}<0.5			2.0	uA
Off state leakage from A1 to B01 (or B11)	I_A	V_A = 5.5V , $V_{B01(or\ B11)}$ = 0V			±2.0	uA
Off state leakage from A2 to B02 (or B12)	I_A	V_A = 5.5V , $V_{B02(or\ B12)}$ = 0V			±2.0	uA
On-Resistance	R_{ON1}	V_A=0 ~ 0.5V, I_A=30mA		3.0	3.5	Ω
	R_{ON2}	V_A=0.5 ~ 2.0V, I_A=30mA		3.6	3.9	Ω
	R_{ON3}	V_A=2.0 ~ 4.0V, I_A=30mA		2.5	3.5	Ω
	R_{ON4}	V_A=4.0 ~ 5.5V, I_A=30mA		1.5	1.8	Ω
On-Resistance Flatness	R_{FLAT1}	V_A=0 ~ 0.5V, I_A=30mA		0.7		Ω
	R_{FLAT2}	V_A=0.5 ~ 2.0V, I_A=30mA		0.5		Ω
	R_{FLAT3}	V_A=2.0 ~ 4.0V, I_A=30mA		1.6		Ω
	R_{FLAT4}	V_A=4.0 ~ 5.5V, I_A=30mA		0.3		Ω
On-Resistance Matching Between Channels	Δ R_{ON}	V_A=0~5.5V, I_A=30mA		0.1	0.2	Ω
AC Characteristics (Normal Speed Channel)						
Turn-On Time	T_{ON}	V_A=1.5V, C_L=35pF, RL=50Ω		200		nS
Turn-Off Time	T_{OFF}	V_A=1.5V, C_L=35pF, R_L=50Ω		200		nS
Break-Before-Make time	T_{BBM}	V_A=1.5V, C_L=35pF, R_L=50Ω		500		nS
-3dB Bandwidth	BW	R_L=50Ω, C_L=0pF		600		MHZ
Off isolation	OIRR	F=1KHz, R_L=50Ω		-81		dB
		F=10KHz, R_L=50Ω		-80		dB
Crosstalk	Xtalk	F=1KHz, R_L=50Ω		-83		dB
		F=10KHz, R_L=50Ω		-82		dB
Total Harmonic Distortion	THD	F=20Hz to 20KHz V_A=600mVp-p @R_L=32Ω,		-80		dB
Capacitance (Normal Speed Channel)						
Off capacitance	C_{OFF}	F=100KHz, VCC=3.3		5		pF
On capacitance	C_{ON}	F=100KHz, VCC=3.3		7		pF

Notes:

(1) Flatness is defined as the difference between maximum and minimum value of ON-resistance at the specified analog signal voltage points.

(2) R_{ON} matching between channels is calculated by subtracting the channel with the lowest max Ron value from the channel with the highest max Ron value.

(3) Crosstalk is inversely proportional to source impedance

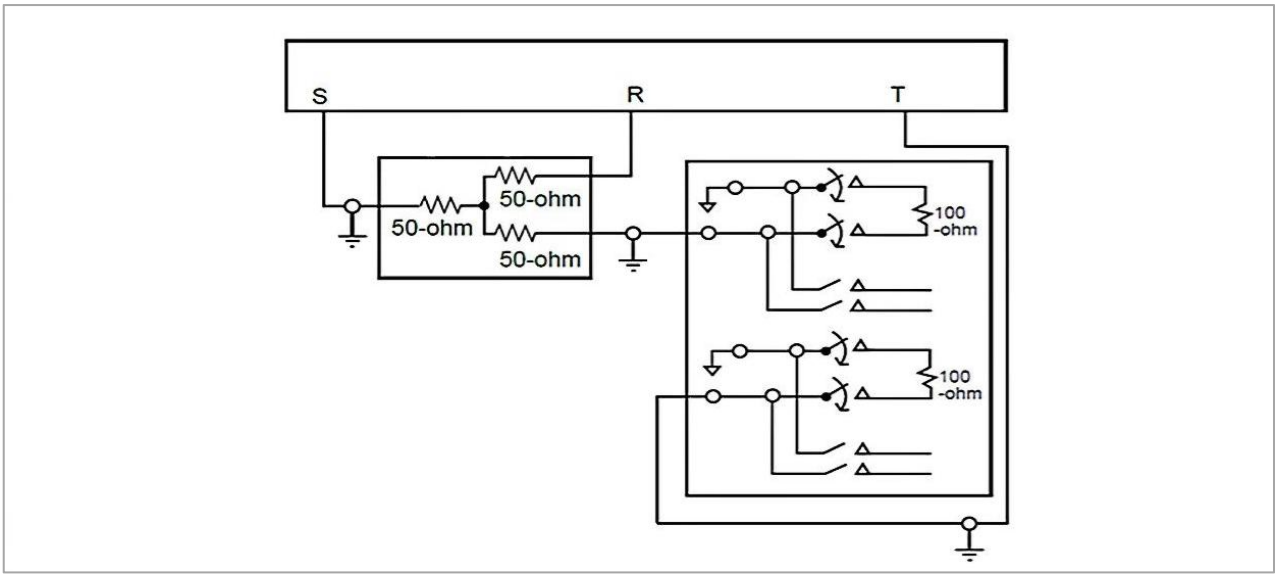


Fig.1 Crosstalk Setup

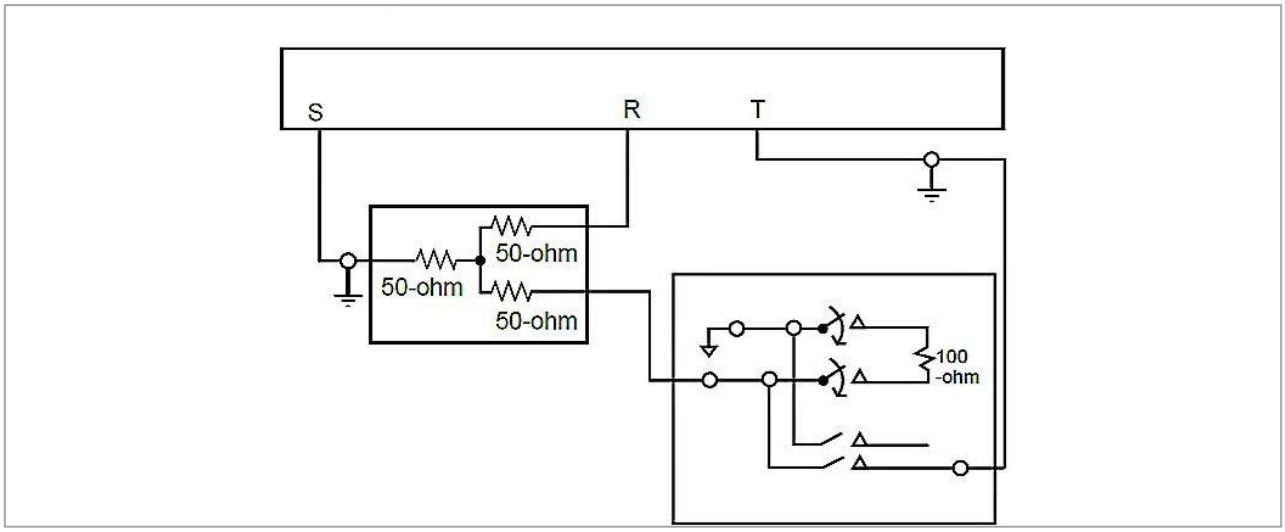
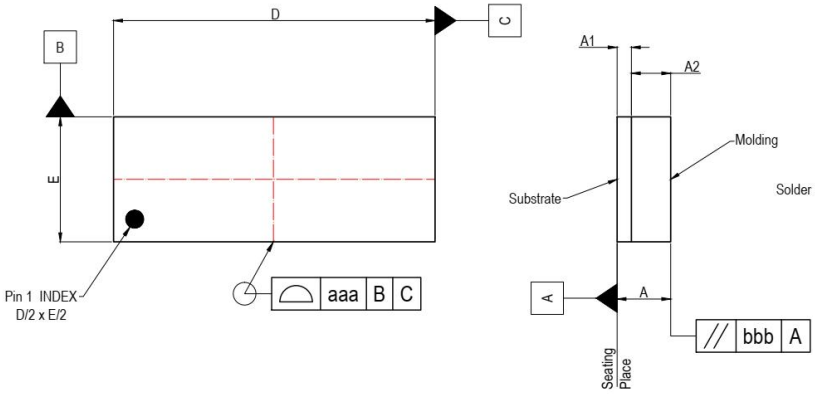


Fig.2 OFF-isolation

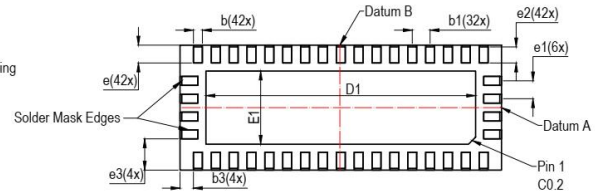
11.Package Outline Dimensions(All dimensions in mm.)

Package Type: LGA42-3.5x9.0x0.75



Top View

Side View



Bottom View

Dimensional References							unit: mm
Ref.	MIN	NOR	MAX	Ref.	MIN	NOR	MAX
A	0.700	0.750	0.800	b	0.200	0.250	0.300
A1	0.170	0.200	0.230	e	0.450	0.500	0.550
A2	0.500	0.550	0.600	b1	0.450	0.500	0.550
D	8.900	9.000	9.100	e1	0.450	0.500	0.550
E	3.400	3.500	3.600	e2	0.400	0.450	0.500
D1	7.500	7.550	7.600	b3	0.325	0.375	0.425
E1	2.000	2.050	2.100	e3	0.825	0.875	0.925
aaa		0.100		bbb		0.200	

Note:
1. All dimension are in millimeter.
2. Dimension 'A' includes package warpage.
3. Exposed metallized pads are Cu pads with surface finish protection.

12.Important Notice And Disclaimer

● We reserves the right to change the instruction manual without prior notice.

● Any semiconductor product has a certain possibility of failure or malfunction under specific conditions. The buyer is responsible for complying with safety standards and taking safety measures when using our products for system design and overall manufacturing to avoid potential failure risks that may cause personal injury or property damage.

● The improvement of product quality is endless, our company will be dedicated to provide customers with better products.