Dual 2:1 USB2.0 Mux/De-Mux

1.Description

The FSW7227A is a bidirectional low-power dual port, high-speed, USB 2.0 analog switch with integrated protection for USB Type-C™ systems. The device is configured as a dual 2:1 or 1:2 switch. It is optimized for use with the USB 2.0 DP/DM lines in a USB Type-C™ system. GPIO controls of SEL and $\overline{EN}$ are 1.8V logic compatible.

The FSW7227A is available in UQFN 1.4x.18-10L and MSOP10 with Pb-free and Halogen-free making it a perfect candidate for mobile and space constrained applications.

2.Features

- Supply Range 1.8V to 5.5 V
- Differential 2:1 or 1:2 Switch/Multiplexer
- Low R_{ON} of 11 Ω Typical
- Low Crosstalk: -63dB @100MHz
- -3dB Bandwidth: 1.4GHz
- Off Isolation: -33dB @100MHz
- Break-Before-Make Switching
- Temperature Range of -40°C to 85°C

3.applications

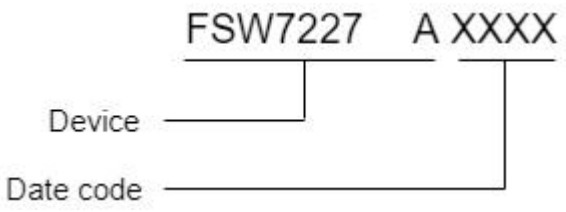
- Anywhere a USB Type-C™ or Micro-B Connector is Used
- USB 2.0 Signal Routing
- Digital Cameras and Camcorders
- Portable Instrumentation
- Set-Top Box
- PADS the withstand USB devices
- Mobile Phones, Tablets and Notebooks

4.Order Information

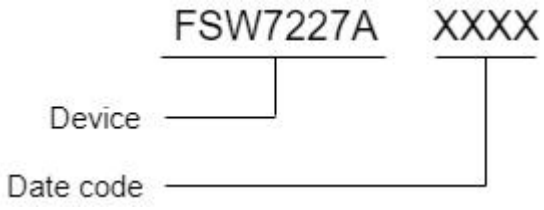
Device	Package	Specified Temperature Range	Ordering Number	Packing Option
FSW7227A	UQFN 1.4x1.8-10L	-40℃ to +85℃	FSW7227AYUWQ10G/TR	Tape and Reel, 3000
	MSOP10	-40℃ to +85℃	FSW7227AYMS10G/TR	Tape and Reel, 3000

5.Marking Information

(1) Package Type: UQFN 1.4x1.8-10L



(2) Package Type: MSOP10



Note:

XXXX -For example, "2503" represens the third week of the 25th year.

6.Pin Configuration

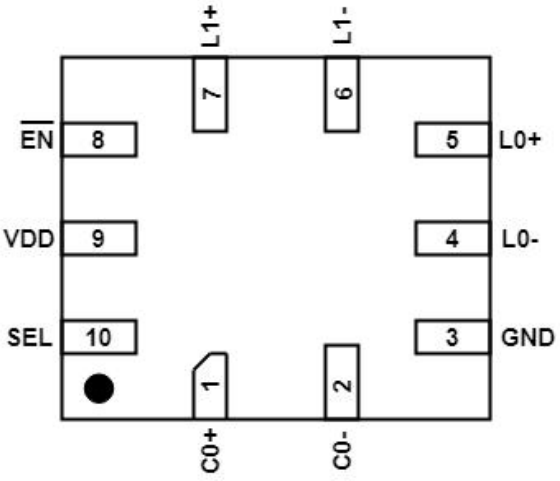


Figure 1. UQFN 1.4x1.8-10L

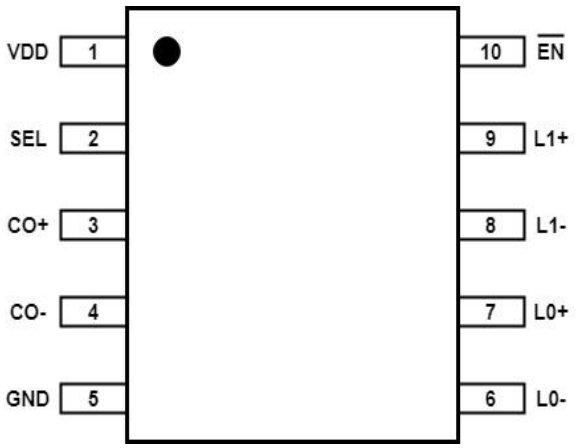


Figure 2. MSOP10

7.Pin Description

UQFN1.4x1.8-10L	MSOP10	Pin Name	Signal Type	Description
1	3	C0+	I/O	Signal I/O, Common Port
2	4	C0-	I/O	Signal I/O, Common Port
7	9	L1+	I/O	Signal I/O, Channle 1
6	8	L1-	I/O	Signal I/O, Channle 1
5	7	L0+	I/O	Signal I/O, Channle 0
4	6	L0-	I/O	Signal I/O, Channle 0
10	2	SEL	I	Operation Model Select (when SEL=0: C0→L0, when SEL=1: C0→L1)
8	10	_EN	I	_EN=1, Power Down is Enabled
9	1	VDD	PWR	Positive Supply Voltage
3	5	GND	GND	Power Ground

8.Truth Table

Function	SEL	_EN
C0+/- to L0+/-	L	L
C0+/- to L1+/-	H	L
All Switches Hi-Z	X	H

9.Typical Application

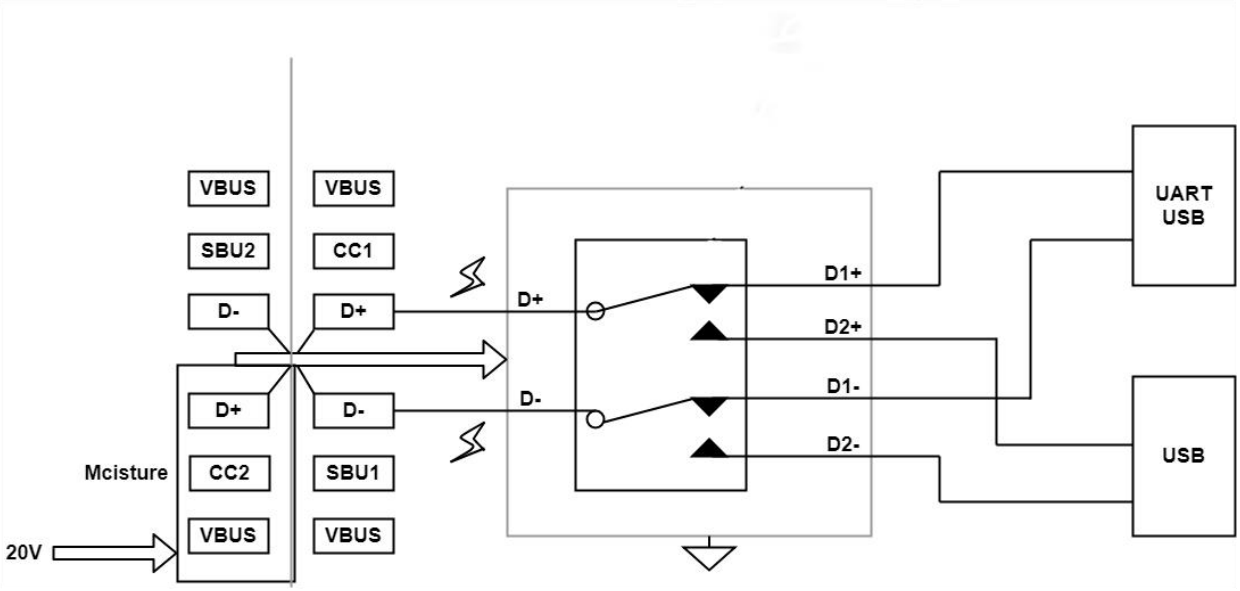


Figure 3. FSW7227A Application circuit

In addition, considering the power consumption requirements of portable products, FSW7227A is designed to minimize static power consumption. As shown in Figure 5 below, FSW7227A integrates pull-down resistance on both SEL and / OE pins. The weak pull-down resistance on the SEL pin saves power and ensures that channel 1 is opened in the default state, and the weak pull-down resistance on the OE pins ensures that the chip can work after power on.

10.Functional Diagram

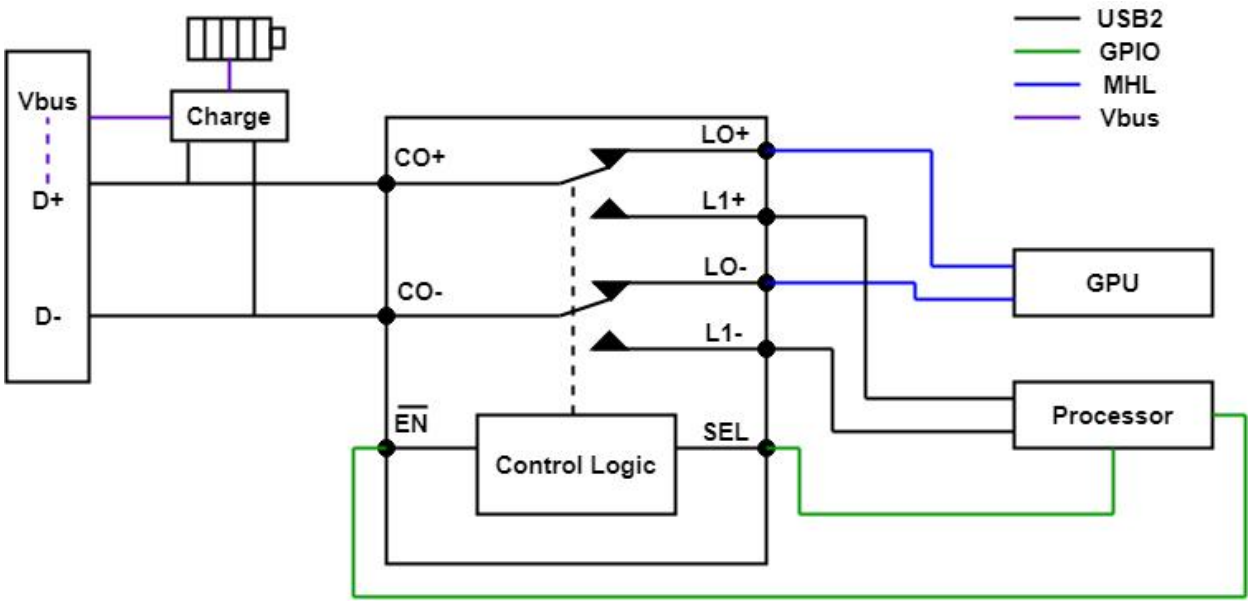


Figure 4. Function Diagram

FSW7227A is a high-speed, low-power double knife/double throw (DPDT) analog switch, supporting power supply from 1.8V to 5.5V. FSW7227A Designed to switch high-speed USB 2.0 signals in handheld devices (such as mobile phones, digital cameras, and laptops, with hubs or controllers).

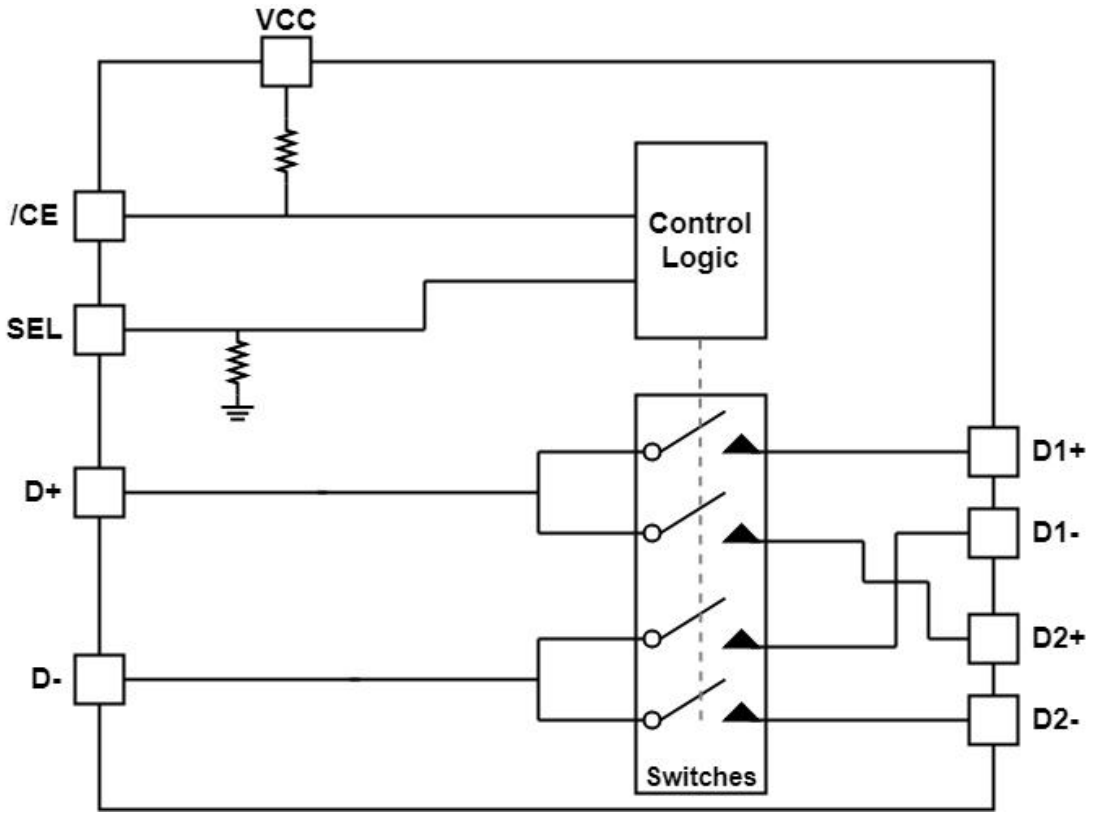


Figure 5. Internal function diagram

11.Electrical Characteristics

(T_A=25°C, V_{DD}=3.3V, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
Supply Voltage Range	V_{DD}		1.8	3.3	5.5	V
Supply Current	I_{CC}	_EN=V_{DD},V_{DD}=5.5V		0.1	1	uA
		_EN=0,V_{DD}=2.5V,V_{SEL}=0 or 1			50	
		_EN=0,V_{DD}=3.3V,V_{SEL}=0 or 1			70	
		_EN=0,V_{DD}=5.5V,V_{SEL}=0 or 1			120	
SEL DIGITAL INPUT CONTOL						
control input logic high	V_{IH}	V_{DD}=3.3V	1			V
		V_{DD}=5.5V	1.3			
control input logic low	V_{IL}	V_{DD}=3.3V			0.75	V
		V_{DD}=5.5V			0.9	
pull-down resistance	R_{SEL}	V_{DD}=3.6V,V_{SEL}=0.3V or 3.3V; V_{DD}=5.5V,V_{SEL}=1V or 4.5V; $V_{I/O}$=0		220		kΩ
Control Input Leakage Current	I_{SEL}	V_{DD}=3.6V,V_{SEL}=0.3V,$V_{I/O}$=0			1.6	uA
		V_{DD}=3.6V,V_{SEL}=3.3V,$V_{I/O}$=0			17	
SWITCH ON RESISTANCE AND OFF LEAKAGE						
On-Resistance	R_{ON}	V_{DD}=3.3V,$V_{C0+/-}$=0V~5.5V,I_D=8mA, V_{SEL}=0V or V_{DD}		11	14	Ω
R_{ON} Flatness(1)	R_{FLAT}			0.05	0.17	Ω
R_{ON} Matching Between Channels(2)	ΔR_{ON}			0.7	1	Ω
Channel Off Leakage Current	$I_{L0/L1}$	V_{DD}=3.3V,$V_{L0+/-}$=0.3V or 3.3V, $V_{L1+/-}$=0.3V or 3.3V $V_{C0+/-}$=0V,V_{SEL}=0V or V_{DD}			±50	nA
Power OFF Leakage Current(C0+/C0-)	I_{OFF}	V_{DD}=3.6V,$V_{C0+/-}$=0.3V or 3.3V,$V_{L0/L1}$=0V,V_{SEL}=0V or V_{DD}			±10	nA
SWITCH DYNAMICS						
Off Isolation	O_{ISO}	f=1GHz,R_L=50Ω,Signal=-10dBm		-27		dB
		f=100MHz,R_L=50Ω, Signal=-10dBm		-33		
Crosstalk(3) (Channel-to-Channel)	X_{TALK}	f=1GHz,R_L=50Ω,Signal=-10dBm		-35		dB
		f=100MHz,R_L=50Ω, Signal=-10dBm		-63		
-3dB Bandwidth	BW	R_L=50Ω,Signal=-10dBm		1.4		GHz
Break-Before-Make Delay Time	T_{BBM}	$V_{C0+/-}$=0.4V,R_L=300Ω,C_L=10pF		556		ns
Turn-on Time	t_{ON}	$V_{C0+/-}$=0.4V,R_L=300Ω,C_L=10pF		960		ns
Turn-off Time	t_{OFF}	$V_{C0+/-}$ = 0.4V, R_L=300Ω, CL=10pF		32		ns

Note:

(1) Flatness is defined as the difference between maximum and minimum value of ON-resistance at the specified analog signal voltage points.

(2) R_{ON} matching between channels is calculated by subtracting the channel with the lowest max Ron value from the channel with the highest max Ron value.

(3) Crosstalk is inversely proportional to source impedance.

12.Typical Performance Curves

T_A=25°C, V_{DD}=3.3V, unless otherwise noted

Fig 7. Switch Bandwidth

Fig 8. Switch Cross-Talk

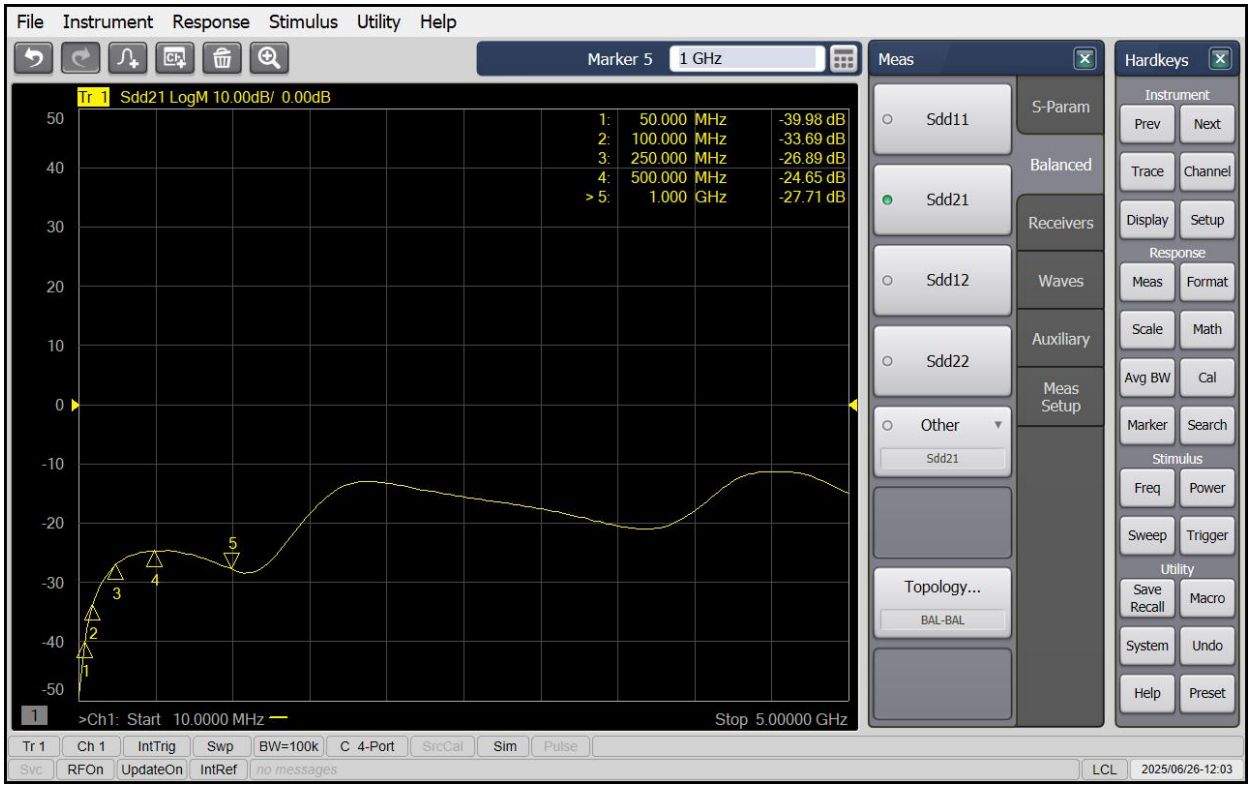
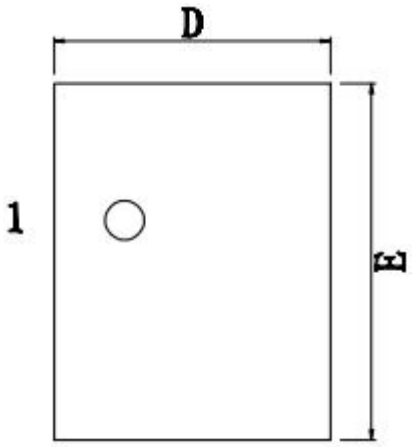


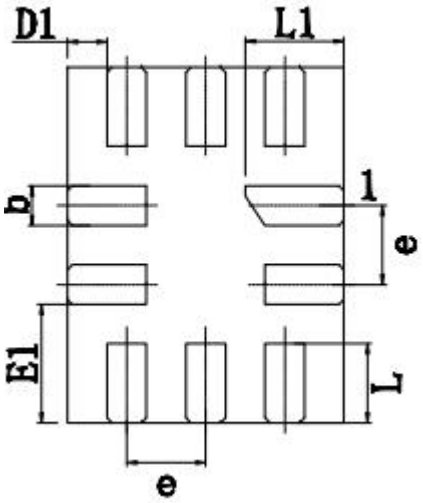
Fig 9. Switch Off Isolation

13.Package Outlihne Dimensions

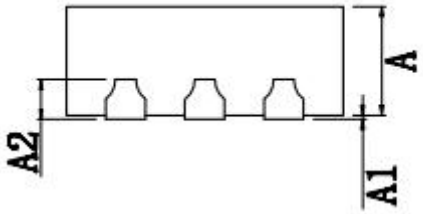
(1) Package Type: UQFN 1.4x1.8 -10L(All dimensions in mm.)



top view



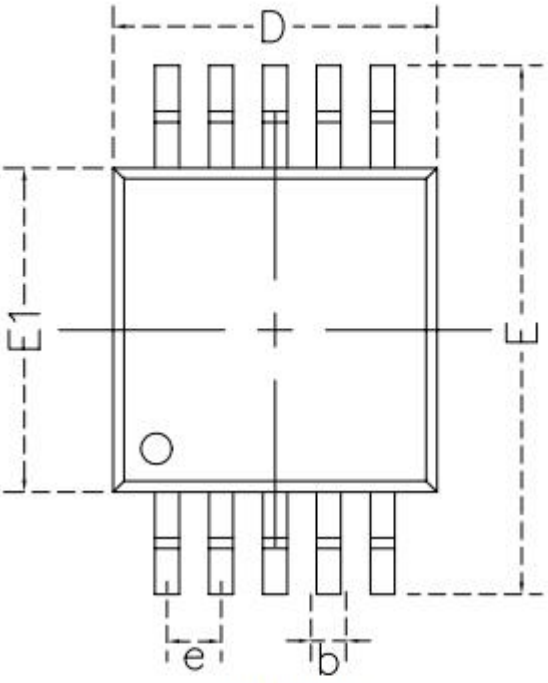
bottom view



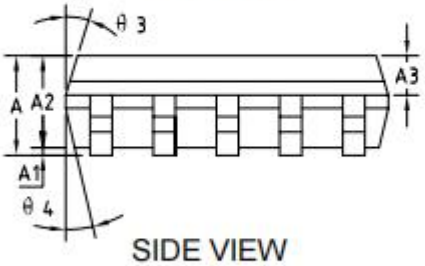
vertical view

SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0.00	-	0.05
A2		0.203 TYP	
b	0.15	0.20	0.25
D	1.35	1.40	1.45
D1		0.20 REF	
E	1.75	1.80	1.85
E1		0.60 REF	
e		0.40 RSC	
L	0.35	0.40	0.45
L1	0.45	0.50	0.55

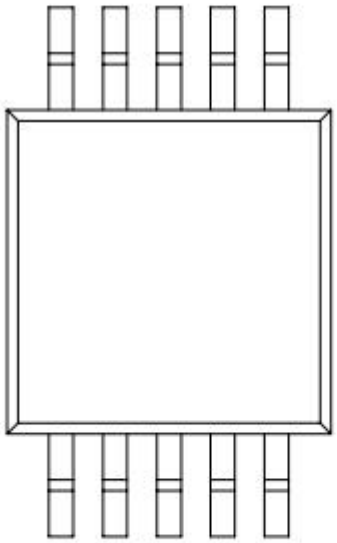
(2) Package Type: MSOP10



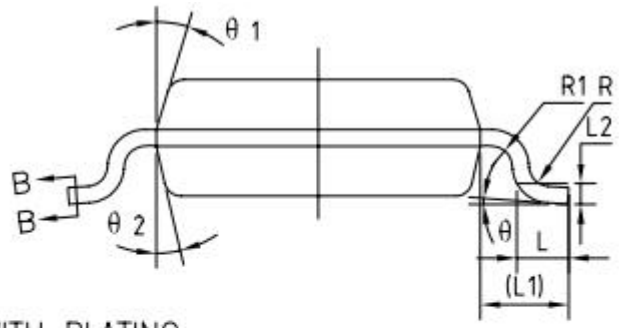
TOP VIEW

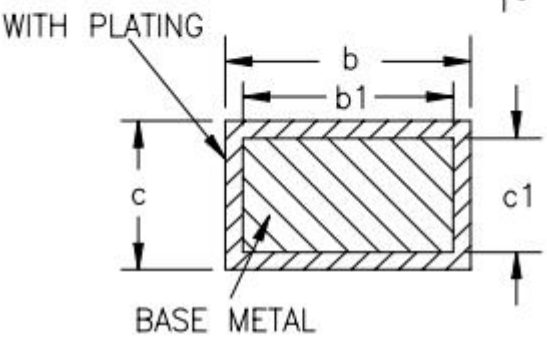


SIDE VIEW



BOTTOM VIEW





SYMBOL	MIN	NOM	MAX
A	–	–	1.10
A1	0	–	0.15
A2	0.75	0.85	0.95
A3	0.25	0.35	0.39
b	0.18	0.225	0.27
b1	0.17	0.20	0.23
c	0.154	0.177	0.20
c1	0.144	0.152	0.16
D	2.90	3.00	3.10
e	0.40	0.50	0.60
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
L	0.40	0.60	0.80
L1	0.95REF		
L2	0.25BSC		
R	0.07	--	--
R1	0.07	--	--
θ	0°	--	8°
θ1	9°	12°	15°
θ2	9°	12°	15°
θ3	9°	12°	15°
θ4	9°	12°	15°

NOTES:
1.All DIMENSIONS REFER TO JEDEC STANDARD MO-137E
2.DIMENSION D DOES NOT INCLUDE MOLD FLASH
3.DIMENSION E1 DOSE NOT INCLUDE MOLD FLASH
4.FLASH OR PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE.

14.Important Notice And Disclaimer

- We reserves the right to change the instruction manual without prior notice.
- Any semiconductor product has a certain possibility of failure or malfunction under specific conditions. The buyer is responsible for complying with safety standards and taking safety measures when using our products for system design and overall manufacturing to avoid potential failure risks that may cause personal injury or property damage.
- The improvement of product quality is endless, our company will be dedicated to provide customers with better products.

15.Version Modification Record

Version Number	Revision
first edition	
V0.4	1. Update the PACKAGE OUTLIHNE DIMENSIONS on page 9 &10. 2. Update the PACKAGE MARKING INFORMATION on page2.