1.Description

The FIF232 device is a dual driver/receiver that includes a capacitive voltage generator to supply TIA/EIA-232-F voltage levels from a single 5V supply.Each receiver converts TIA/EIA-232-F inputs to 5V TTL/CMOS levels.These receivers have a typical threshold of 1.3V,a typical hysteresis of 0.5V,and can accept ±30V inputs.Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels.

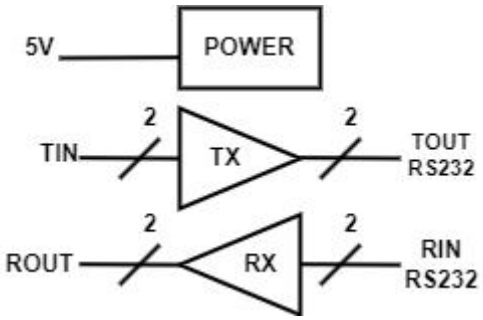
2.Features

- Meets or Exceeds TIA/EIA-232-F and ITU Recommendation V.28
- Operates From a Single 5V Power Supply With 1.0μF Charge-Pump Capacitors
- Operates up to 120 kbit/s
- Two Drivers and Two Receivers
- ±30V Input Levels
- Low Supply Current: 8mA Typical
- ESD Protection Exceeds JESD22 2000V Human-Body Model (A114-A)
- Upgrade With Improved ESD (15 KV HBM) and 0.1μF Charge-Pump Capacitors is Available With the 202 Device

3.Applications

- TIA/EIA-232-F
- Battery-Powered Systems
- Terminals
- Modems
- Computers

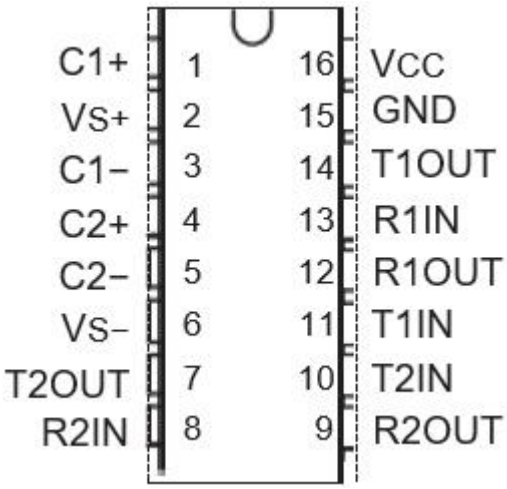
4.Simplified Schematic



5.Order Information

Mode	Package	BODY SIZE	Ordering Number	Packing Option
FIF232	SOP16	9.90 mm × 3.91 mm	FIF232YSOP16G/TR	Tape and Reel,4000
	WSOP16	10.30 mm × 7.50 mm	FIF232YWSOP16G/TR	Tape and Reel,1500
	DIP16	19.30 mm × 6.35 mm	FIF232YDIP16G/TR	Tape and Reel

6.Pin Configuration



7.Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
C1+	1	-	Positive lead of C1 capacitor
VS+	2	O	Positive charge pump output for storage capacitor only
C1-	3	-	Negative lead of C1 capacitor
C2+	4	-	Positive lead of C2 capacitor
C2-	5	-	Negative lead of C2 capacitor
VS-	6	O	Negative charge pump output for storage capacitor only
T2OUT,T1OUT	7,14	O	RS232 line data output (to remote RS232 system)
R2IN,R1IN	8,13	I	RS232 line data input (from remote RS232 system)
R2OUT,R1OUT	9,12	O	Logic data output (to UART)
T2IN,T1IN	10,11	I	Logic data input (from UART)
GND	15	-	Ground
V_{CC}	16	-	Supply Voltage, Connect to external 5V power supply

8.Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter		MIN	MAX	UNIT
V_{CC}	Input Supply voltage range(2)		-0.3	6	V
V_{S+}	Positive output supply voltage range		V_{CC}-0.3	15	V
V_{S-}	Negative output supply voltage range		-0.3	-15	V
V_I	Input voltage range	T1IN, T2IN	-0.3	V_{CC}+0.3	V
		R1IN, R2IN		±30	V
V_O	Output voltage range	T1OUT,T2OUT	V_{S-}-0.3	V_{S+}+0.3	V
		R1OUT,R2OUT	-0.3	V_{CC}+0.3	V
	Short-circuit duration	T1OUT, T2OUT	Unlimited		
T_J	Operating virtual junction temperature			150	°C

Notes:

(1)Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device.These are stress ratings only,and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied.Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network GND.

9.Handling Ratings

Symbol	Parameter		MIN	MAX	UNIT
T_{stg}	Storage temperature range		-65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	0	1000	

Notes:

JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

10.Recommended Operating Conditions

Symbol	Parameter	MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage (T1IN,T2IN)	2			V
V_{IL}	Low-level input voltage (T1IN,T2IN)			0.8	V
R1IN	Receiver input voltage			±30	V
R2IN					
T_A	Operating free-air temperature	-20		85	°C

11.Electrical Characteristics----Device

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6)

Symbol	Parameter	TEST CONDITIONS (1)	MIN	TYP(2)	MAX	UNIT
I_{CC}	Supply current	V_{CC} = 5.5V, all outputs open, T_A= 25°C		8	10	mA

Notes:

(1) Test conditions are C1–C4 =1pF at V_{CC} = 5V±0.5V.

(2) All typical values are at V_{CC} = 5V, and T_A = 25°C.

12.Electrical Characteristics----Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

Symbol	Parameter		TEST CONDITIONS (1)	MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	T1OUT,T2OUT	R_L = 3 kΩ to GND	5	7		V
V_{OL}	Low-level output voltage (3)	T1OUT,T2OUT	R_L = 3 kΩ to GND		-7	-5	V
r_O	Output resistance	T1OUT,T2OUT	V_{S+} = V_{S-} = 0, V_O = ±2 V	300			Ω
I_{OS}(4)	Short-circuit output current	T1OUT,T2OUT	V_{CC} = 5.5 V, V_O = 0 V		±10		mA
I_{IS}	Short-circuit input current	T1IN, T2IN	V_I = 0			200	uA

Notes:

(1)Test conditions are C1–C4=1 pF at V_{CC}=5 V±0.5V

(2)All typical values are at V_{CC}=5 V,T_A=25°C.

(3)The algebraic convention,in which the least-positive(most negative)value is designated minimum,is used in this data sheet for logic voltage levels only.

(4)Not more than one output should be shorted at a time.

13.Electrical Characteristics----Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

Symbol	Parameter		TEST CONDITIONS (1)	MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	T1OUT,T2OUT	I_{OH} = – 1 mA	3.5			V
V_{OL}	Low-level output voltage (3)	T1OUT,T2OUT	I_{OL} = 3.2 mA			0.4	V
V_{IT+}	Receiver positive-going input threshold voltage	R1IN, R2IN	V_{CC} = 5 V, T_A = 25°C		1.7	2.4	V
V_{IT-}	Receiver negative-going input threshold voltage	R1IN, R2IN	V_{CC} = 5 V, T_A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis voltage	R1IN, R2IN	V_{CC} = 5 V	0.2	0.5	1	V
r_I	Receiver input resistance	R1IN, R2IN	V_{CC} = 5 V, T_A = 25°C	3	5	7	kΩ

Notes:

(1)Test conditions are C1–C4=1pF at V_{CC}=5 V±0.5 V.

(2)All typical values are at V_{CC}=5V,T_A=25°C.

(3)The algebraic convention,in which the least-positive(most negative)value is designated minimum,is used in this data sheet for logic voltage levels only.

14.Switching Characteristic

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

Symbol	Parameter	TEST CONDITIONS (1)	MIN	TYP	MAX	UNIT
SR	Driver slew rate	R_L = 3kΩ to 7kΩ , see Figure 4			30	V/ps
SR(t)	Driver transition region slew rate	see Figure 5		3		V/ps
	Data rate	One TOUT switching		120		kbit/s
$t_{PLH®)}$	Receiver propagation delay time, low-to high-level output	TTL load, see Figure 3		500		ns
$t_{PHL®)}$	Receiver propagation delay time, high-to low-level output	TTL load, see Figure 3		500		ns

Notes:

(1)Test conditions are C1–C4=1pF at V_{CC}=5V±0.5V.

15.Typical Characteristics

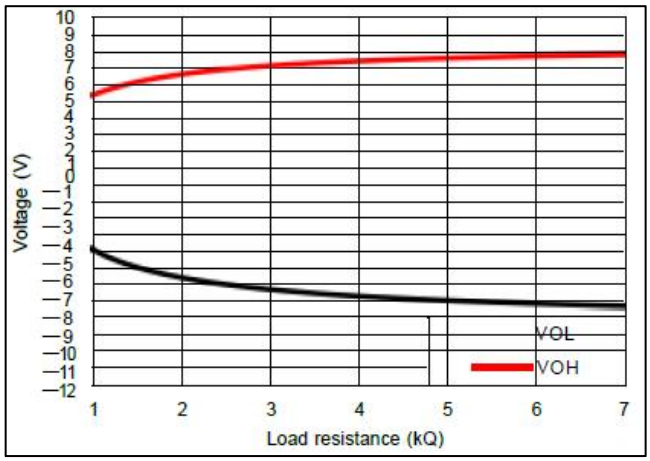


Figure 1. TOUT VOH & VOL vs Load Resistance, Both Drivers Loaded

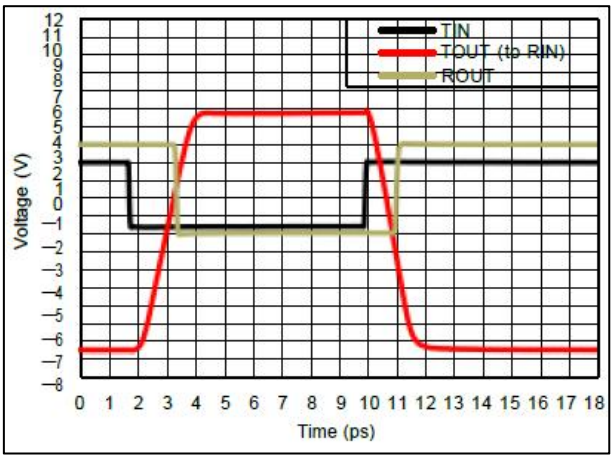


Figure 2. Driver to Receiver Loop back Timing Waveform

16.Parameter Measurement Information

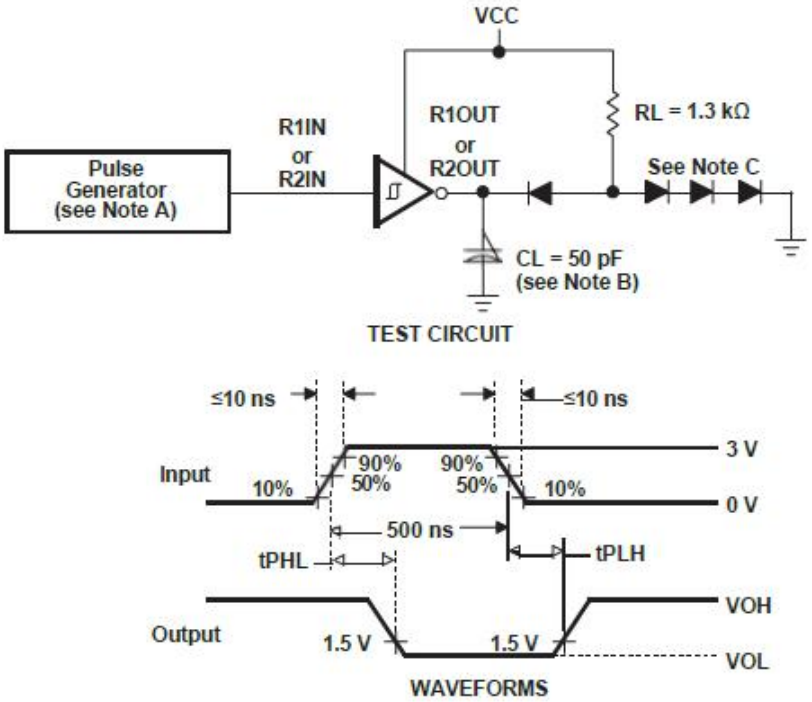


Figure 3. Receiver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements

A. The pulse generator has the following characteristics: Z_O = 50Q, duty cycle ≤ 50%.

B. CL includes probe and jig capacitance.

C. All diodes are 1N3064 or equivalent.

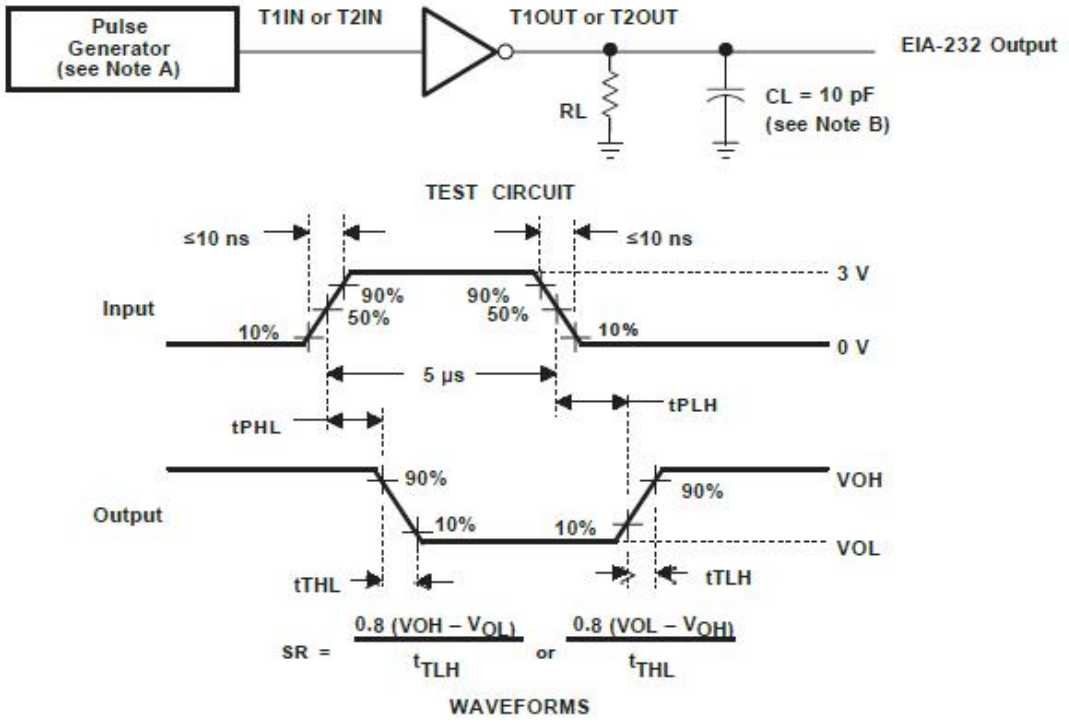


Figure 4. Driver Test Circuit and Wave forms for t_{PHL} and t_{PLH} Measurements (5µs Input)

A. The pulse generator has the following characteristics: Z_O = 50Q, duty cycle ≤ 50%.

B. C_L includes probe and jig capacitance.

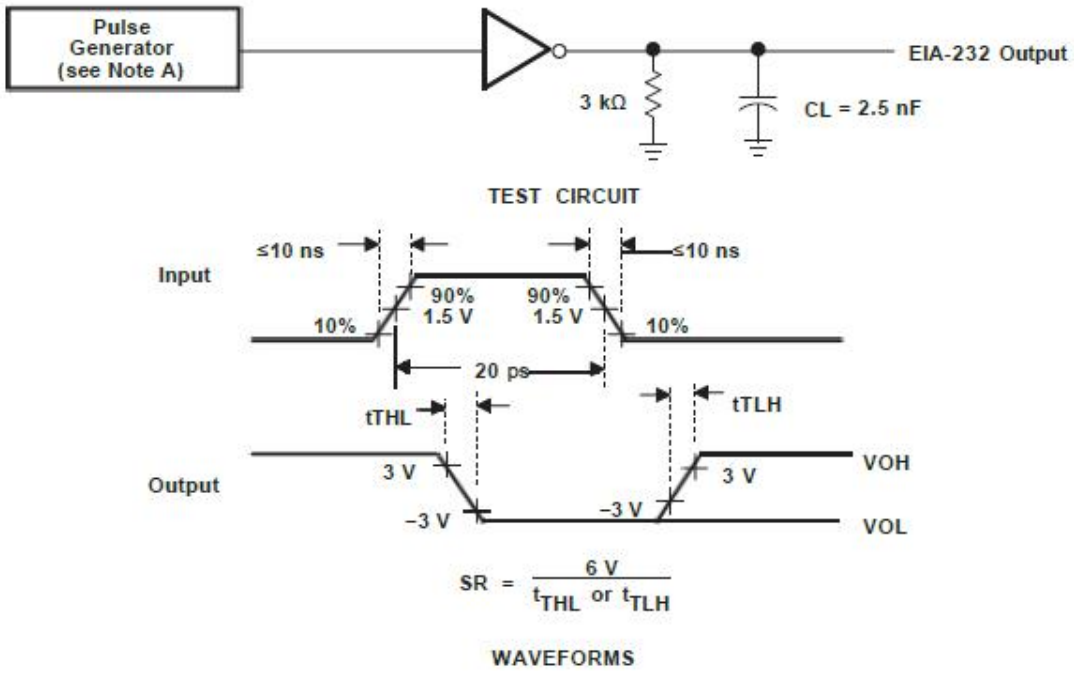


Figure 5. Test Circuit and Wave forms for t_{THL} and t_{TLH} Measurements (20µs Input)

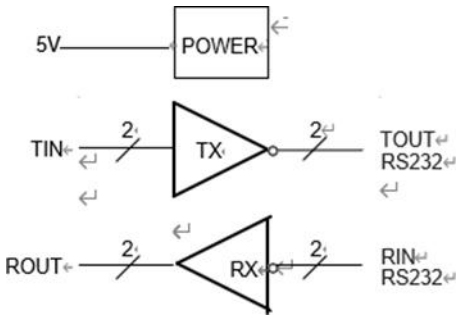
A. The pulse generator has the following characteristics: Z_O = 50Q, duty cycle ≤ 50%.

17.Detailed Description

(1) Overview

The FIF232 device is a dual driver/receiver that includes a capacitive voltage generator using four capacitors to supply TIA/EIA-232-F voltage levels from a single 5V supply. Each receiver converts TIA/EIA-232-F inputs to 5V TTL/CMOS levels. These receivers have a typical threshold of 1.3V, a typical hysteresis of 0.5V, and can accept ±30V inputs. Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels. Outputs are protected against shorts to ground.

(2) Functional Block Diagram



(3) Feature Description

- Power

The power block increases and inverts the 5V supply for the RS232 driver using a charge pump that requires four 1-µF external capacitors.

- RS232 Driver

Two drivers interface standard logic level to RS232 levels. Internal pull up resistors on TIN inputs ensures a high input when the line is high impedance.

- RS232 Receiver

Two receivers interface RS232 levels to standard logic levels. An open input will result in a high output on ROUT.

(4) Device Functional Modes

- V_{CC} powered by 5V

The device will be in normal operation.

- V_{CC} unpowered

When FIF232 is unpowered, it can be safely connected to an active remote RS232 device.

Table 1. Function Table Each Driver(1)

INPUT(TIN)	OUTPUT(TOUT)
L	H
H	L

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

Table 2. Function Table Each Receiver(2)

INPUT(RIN)	OUTPUT(ROUT)
L	H
H	L
OPEN	H

(2) H = high level, L = low level, X = irrelevant, Z = high impedance (off),
Open = disconnected input or connected driver off

18.Application and Implementation

(1) Application Information

For proper operation add capacitors as shown in Figure 6. Pins 9 through 12 connect to UART or general purpose logic lines. EIA-232 lines will connect to a connector or cable.

(2) Typical Application

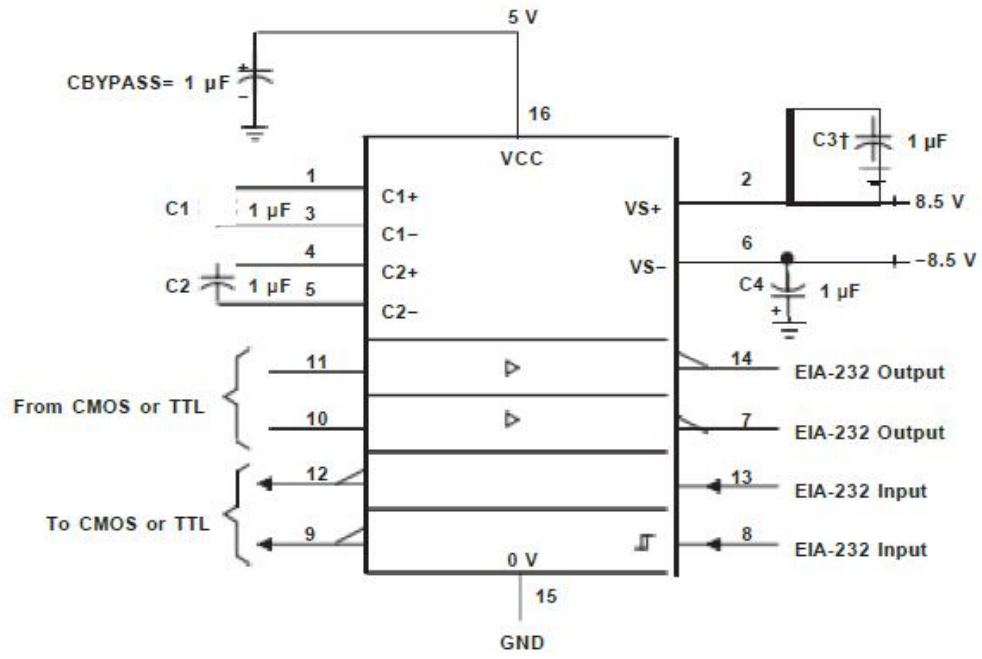


Figure 6. Typical Operating Circuit

C3 can be connected to VCC or GND.

Notes:

A.Resistor values shown are nominal.

B.Non polarized ceramic capacitors are acceptable.If polarized tantalum or electrolytic capacitors are used,they should be connected as shown.In addition to the 1-µF capacitors shown,the 202 can operate with 0.1-µF capacitors.

- Design Requirements

(1) VCC minimum is 4.5V and maximum is 5.5V.

(2) Maximum recommended bit rate is 120Kbps.

- Tailed Design Procedure

Use 1uF tantalum or ceramic capacitors

- Application Curves

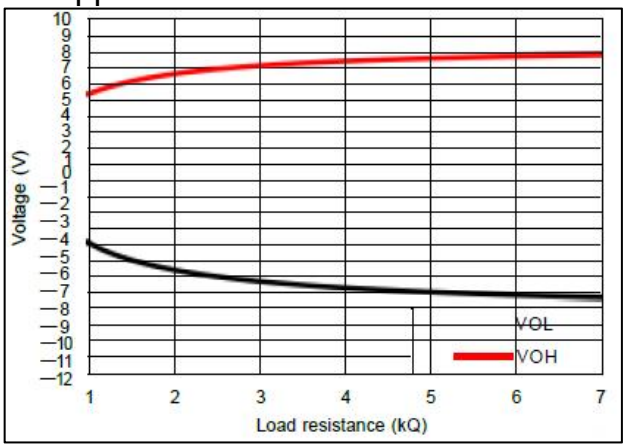


Figure 7. TOUT VOH & VOL vs Load Resistance, Both Drivers Loaded

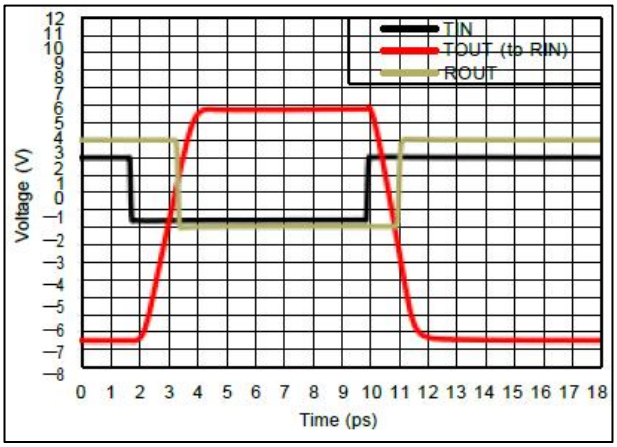


Figure 8. Driver to Receiver Loop back Timing Waveform

19.Power Supply Recommendations

The V_{CC} voltage should be connected to the same power source used for logic device connected to TIN pins. V_{CC} should be between 4.5V and 5.5V.

20.Layout

(1) Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times.

(2) Layout Example

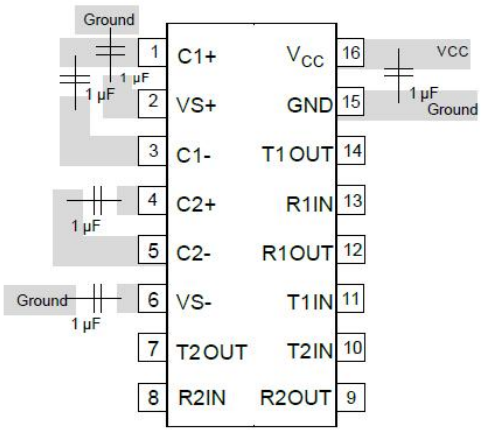
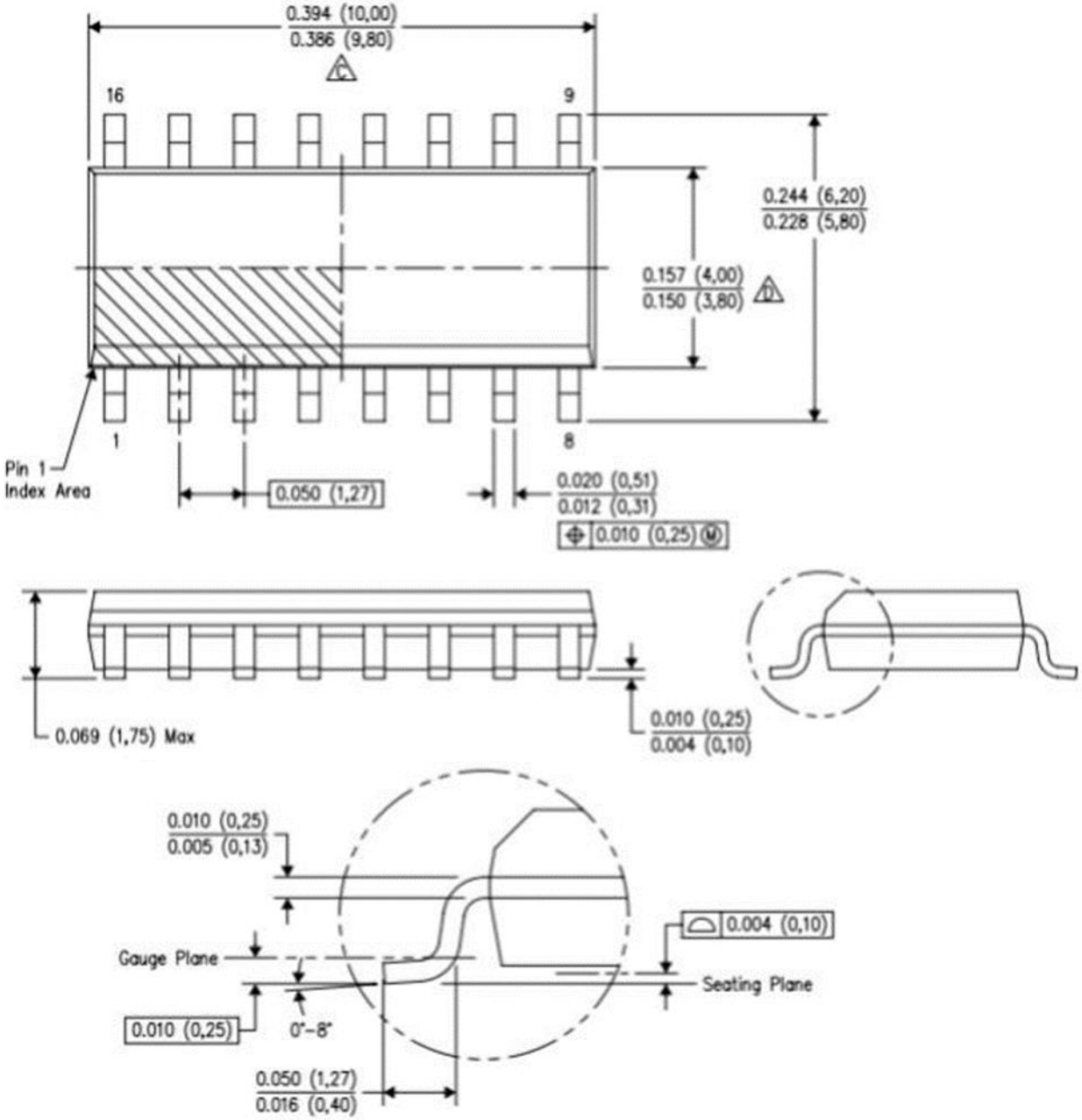


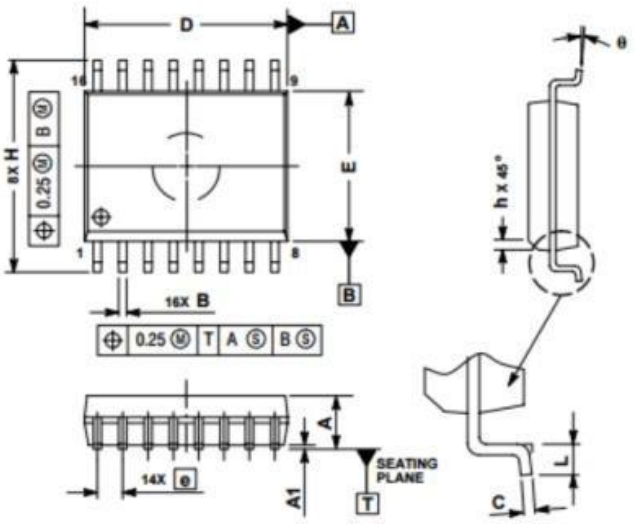
Figure 9. Layout Schematic

21.Package Outline Dimensions

(1) Package Type: SOP16(All dimensions in mm.)



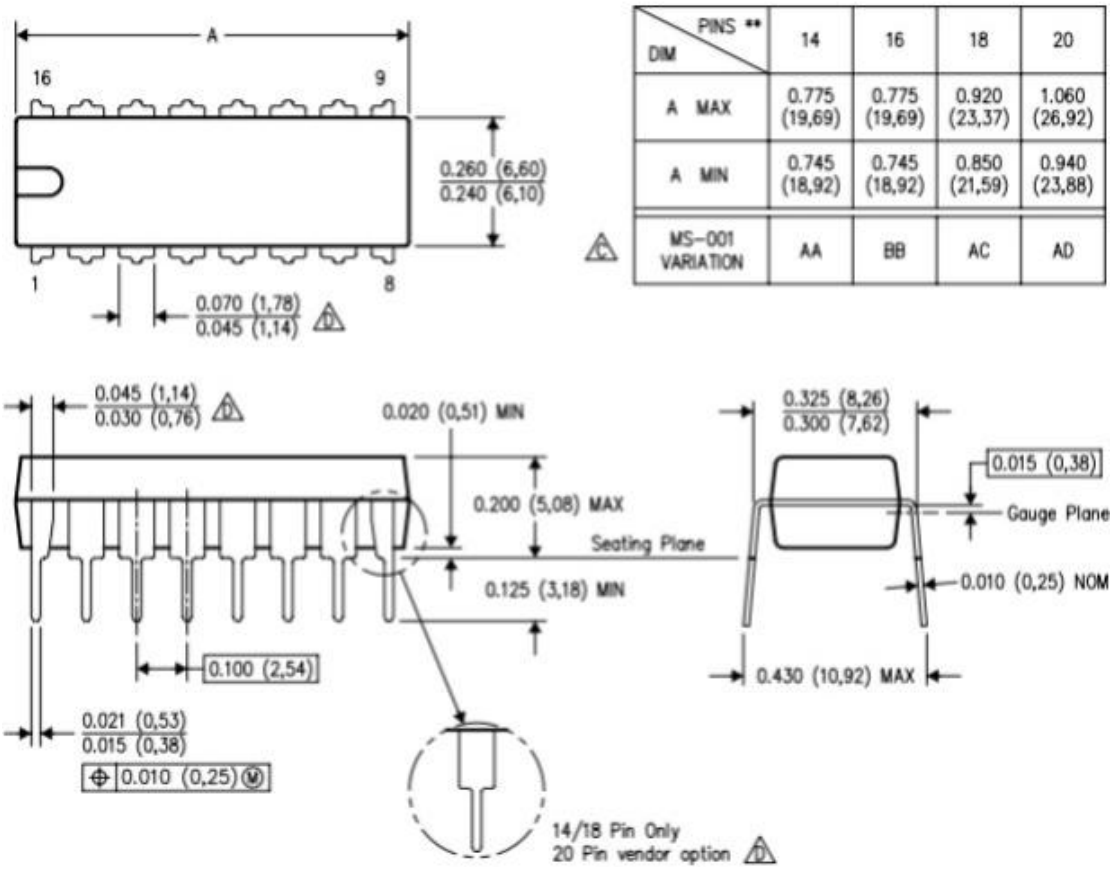
(2) Package Type: WSOP16(All dimensions in mm.)



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
q	0°	7°

(3) Package Type: DIP16(All dimensions in mm.)



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

22.Important Notice And Disclaimer

- We reserves the right to change the instruction manual without prior notice.
- Any semiconductor product has a certain possibility of failure or malfunction under specific conditions. The buyer is responsible for complying with safety standards and taking safety measures when using our products for system design and overall manufacturing to avoid potential failure risks that may cause personal injury or property damage.
- The improvement of product quality is endless, our company will be dedicated to provide customers with better products.

23.Version Modification Record

Version Number	Revision
first edition	
V1.0	1. Update the Important Notice And Disclaimer on page 14. 2. Updated the page layout
V1.1	1. Update Simplified Schematic