9.5Ω, Low Voltage SPDT Analog Switch

Descriptions

The FSW3157A is a single, bidirectional, single-pole/ double-throw (SPDT) CMOS analog switch that is designed to operate from a single 1.8V to 5.5V supply. It features high-bandwidth (-3dB @900MHz) and low on-resistance (9.5Ω TYP), Targeted applications for audio switching.

The FSW3157A features guaranteed on-resistance matching between switches and guaranteed on-resistance flatness over the signal range. This ensures excellent linearity and low distortion when switching audio signals.

The FSW3157A is available in Green SOT23-6 and SOT363 package.

Features

- Supply Voltage Range: 1.8V to 5.5V
- On-Resistance: 9.5Ω (TYP)
- A Overrides VCC to Achieve True Isolation Even When Supply Is Dead
- Low Quiescent Current With Very Wide Supply Range (1.8V ~ 5.5V)
- High Bandwidth: -3dB @900MHz
- Operating Temperature Range: -40℃ to +85℃
- Available in Green SOT23-6 and SOT363 Package

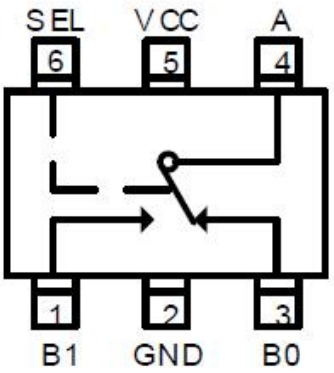
Applications

- Audio, Video, UART, USB2.0 Signal and Supply Routing
- Portable Instrumentation
- Battery-Operated Equipment
- Computer Peripherals
- Cell Phones
- PDAs
- MP3s

Order information

Mode	Package	Specified Temperature range	Ordering Number	Packing Option
FSW3157A	SOT23-6	-40℃ to +85℃	FSW3157AYSOT236G/TR	Tape and Reel,3000
	SOT363	-40℃ to +85℃	FSW3157AYSOT363G/TR	Tape and Reel,3000

Pin Configuration



Pin#	Pin Name	Description
1	B1	Analog/Digital Signal Port (Normally open)
2	GND	Ground
3	B0	Analog/Digital Signal Port (Normally closed)
4	A	Common Signal Port
5	VCC	Single Power Supply
6	SEL	Logic Input Control

Function Table

Logic Input	Function
SEL=0	B0=A
SEL=1	B1=A

Absolute Maximum Ratings(1)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3~6.5	V
Control Input Voltage	V_{SEL}	-0.3~6.5	V
Continuous Current Through A, B0, B1		±100	mA
Peak Current Through A, B0, B1 (pulsed at 1ms 50% duty cycle)		±200	mA
Storage Temperature Range	T_{STG}	-55 ~ 150	℃
Junction Temperature under Bias	T_J	150	℃
Lead Temperature (Soldering, 10 seconds)	T_L	260	℃

Note:

1. “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.

ESD Ratings

		Value	Unit
V(ESD) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommend operating ratings

Parameter	Symbol	Value	Unit
Supply Voltage Operating	V_{CC}	1.8 ~ 5.5	V
Control Input Voltage	V_{SEL}	0 ~ 5.5	V
Input Signal Voltage	V_A	0 ~ 5.5	V
Operating Temperature	T_A	-40 ~ +85	℃

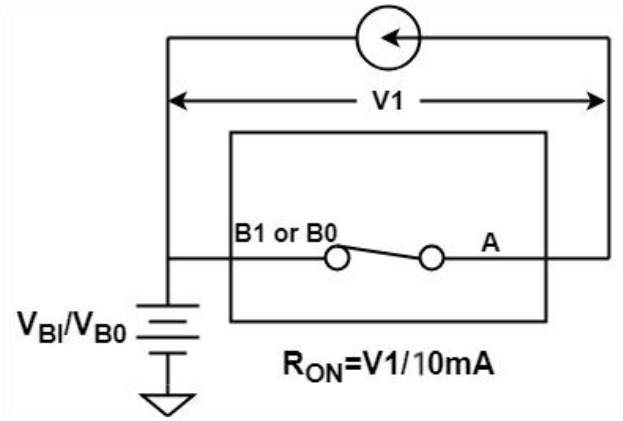
Electrical Characteristics

(V_{CC}= 2.5~5.5V, T_A = +25℃, unless otherwise noted.)

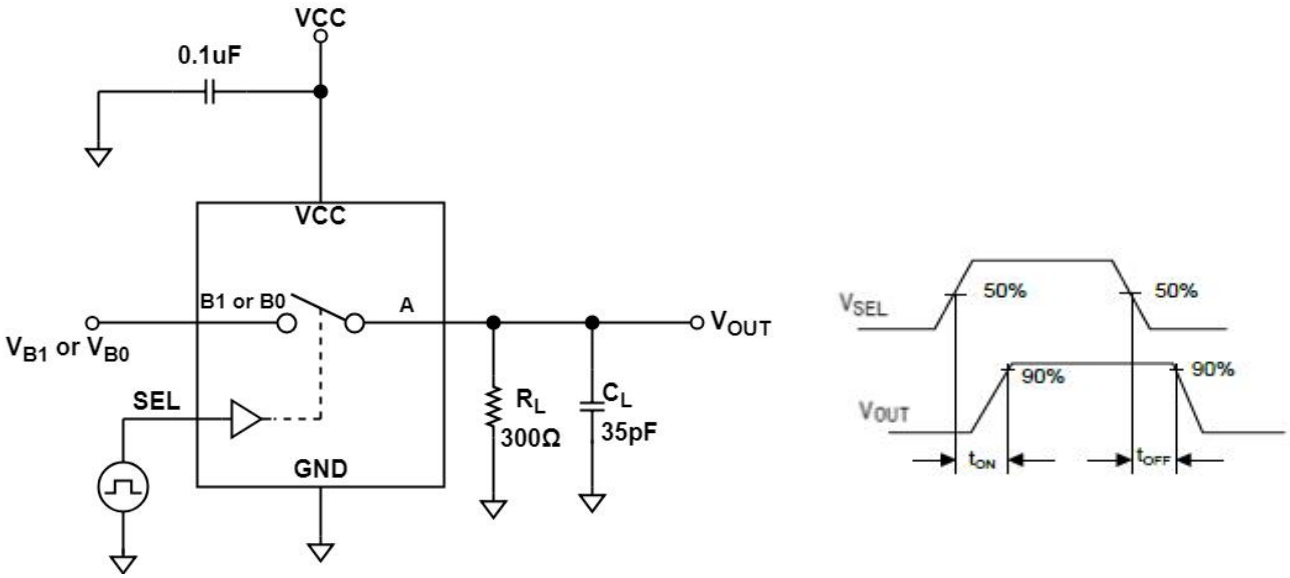
Parameter	Symbol	conditions	Min.	Typ.	Max	Unit
DC CHARACTERISTICS						
Input logic high level	V_{IH}	V_{CC}=2.5V	1			V
		V_{CC}=5V	1.4			
Input logic low level	V_{IL}	V_{CC}=2.5V			0.4	V
		V_{CC}=5V			0.6	
Supply quiescent current	I_{CC}	V_{CC}=2.5V, V_{SEL}=0V or V_{SEL}=V_{CC}			11	uA
		V_{CC}=5.5V, V_{SEL}=0V or V_{SEL}=V_{CC}			25	
Off state leakage from A to B0(or B1)	I_A	V_{CC}=3.6V ,V_A=0.3V or 3.3V; V_{CC}=5.5V ,V_A=1V or 4.5V; V_{SEL}=0V or V_{CC}			±200	nA
On-Resistance	R_{ON}	V_{CC}=3.3V or 5.5V, V_{SEL}=0V or V_{CC}, V_A=0~5.5V, I_A=10mA		9.5	13	Ω
On-Resistance Flatness	R_{FLAT}			0.05	0.1	Ω
On-Resistance Matching Between Channels	ΔR_{ON}			0.05	0.3	Ω
AC CHARACTERISTICS						
Turn-On Time	T_{ON}	V_{CC}=3.3V, V_A=1.5V, V_{SEL}=0V or V_{CC} C_L=33pF, R_L=300Ω		265		ns
Turn-Off Time	T_{OFF}			240		ns

Break-Before-Make time	T_{BBM}			520		ns
-3dB Bandwidth	BW	V_{CC}=3.3V, R_L=50Ω, C_L=5pF		900		MHz
Off isolation	O_{ISO}	F=10MHz, R_L=50Ω, C_L=5pF		-53		dB
		F=500MHz, R_L=50Ω, C_L=5pF		-22		dB

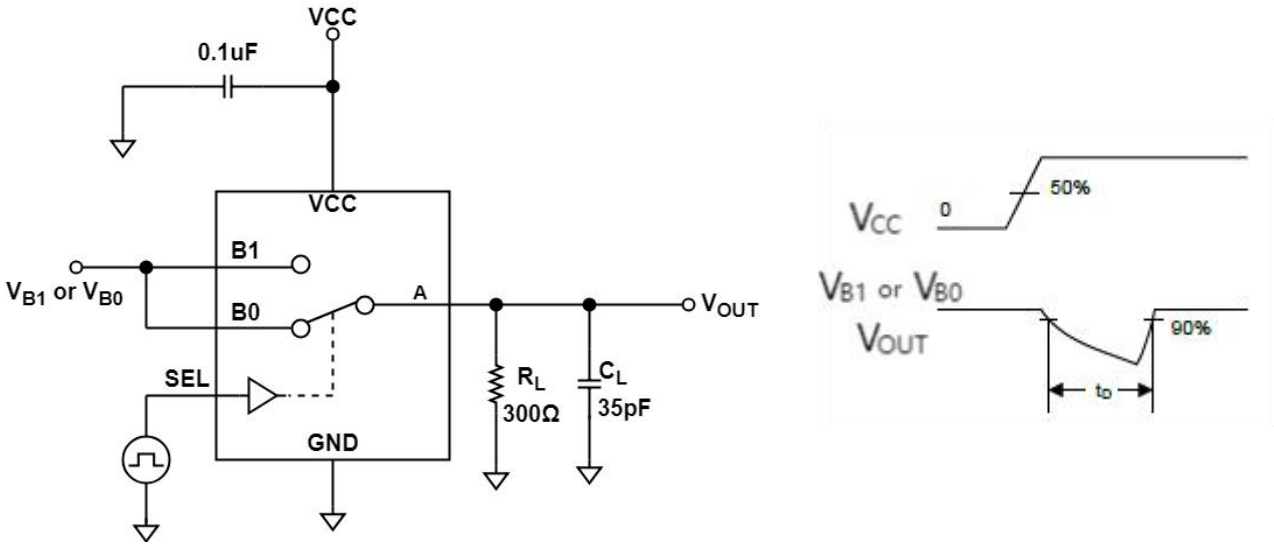
Test Circuits



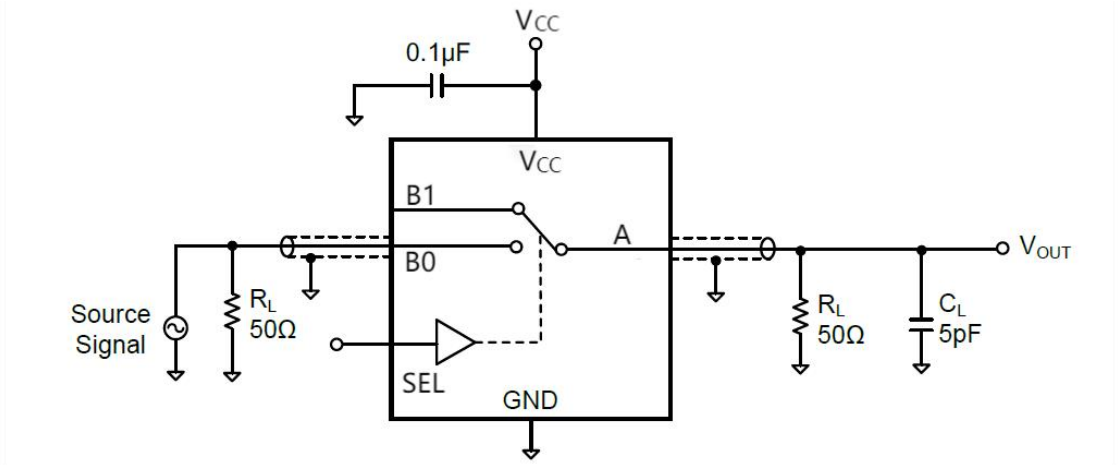
Test Circuit 1. On-Resistance



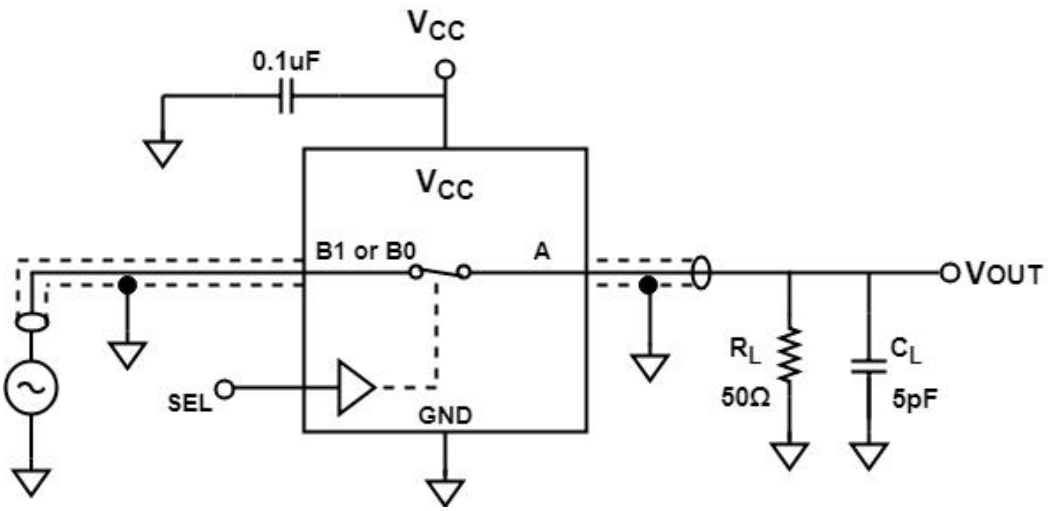
Test Circuit 2. Switching Times



Test Circuit 3. Break-Before-Make Time Delay, t_D



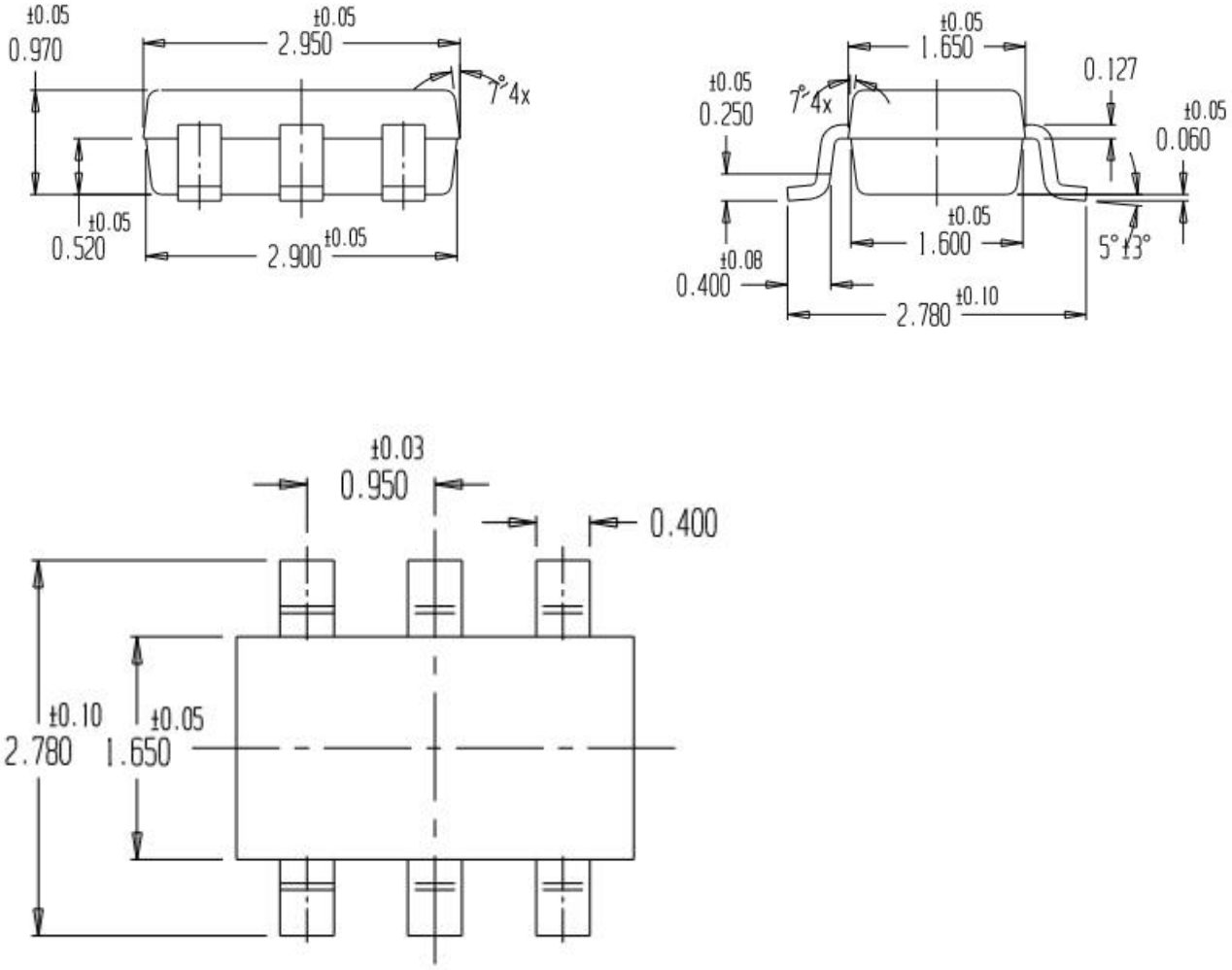
Test Circuit 4. Off Isolation



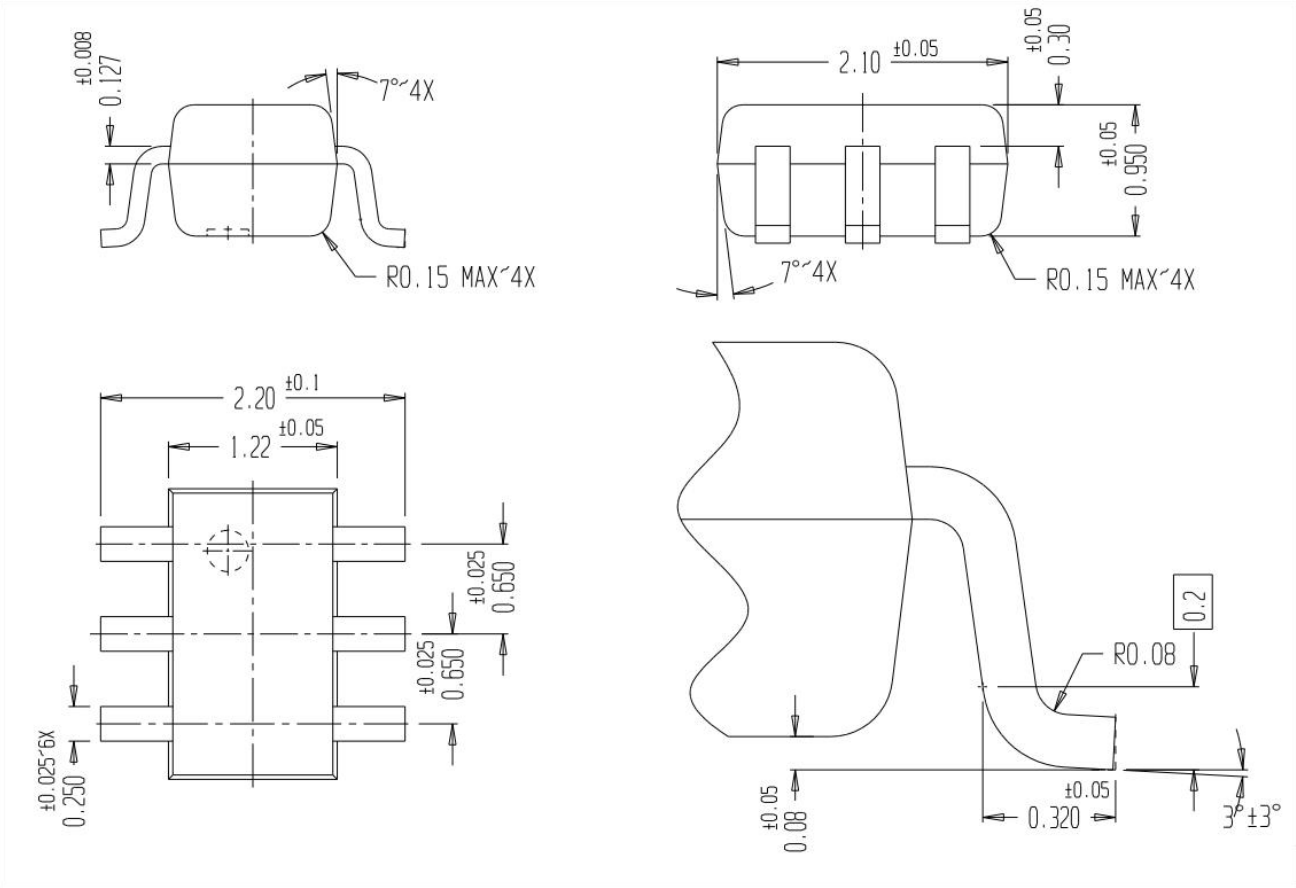
Test Circuit 6. -3dB Bandwidth

Package Outline Dimensions(All dimensions in mm.)

(1) Package Type: SOT23-6



(2) Package Type: SOT363



Important Notice And Disclaimer

- We reserves the right to change the instruction manual without prior notice.
- Any semiconductor product has a certain possibility of failure or malfunction under specific conditions. The buyer is responsible for complying with safety standards and taking safety measures when using our products for system design and overall manufacturing to avoid potential failure risks that may cause personal injury or property damage.
- The improvement of product quality is endless, our company will be dedicated to provide customers with better products.

Version Modification Record

Version Number	Revision	Date
first edition		
V1.0	1. Update the On-Resistance on page 1&3. 2. Update the Off state leakage from A to B0(or B1) on page 3. 3. Update the On-Resistance Matching Between Channels on page 4	2025/05/16