1.5Ω, Low Voltage SPDT Analog Switch

Descriptions

The FSW3157 is a single, bidirectional, single-pole/ double-throw (SPDT) CMOS analog switch that is designed to operate from a single 1.5V to 5.5V supply. It features high-bandwidth (-3dB @700MHz) and low on-resistance (1.5Ω TYP), Targeted applications for audio switching.

The FSW3157 features guaranteed on-resistance matching (0.2Ω MAX) between switches and guaranteed on-resistance flatness over the signal range (0.3Ω TYP). This ensures excellent linearity and low distortion when switching audio signals.

The FSW3157 is available in Green SOT23-6 and SOT363 package.

Features

- Supply Voltage Range: 1.5V to 5.5V
- On-Resistance: 1.5Ω (TYP) When A= 5V
- 1.8V Logic Compatible Control Pin
- A Overrides VCC to Achieve True Isolation Even When Supply Is Dead
- Low Quiescent Current (<2uA) With Very Wide Supply Range (1.5V ~ 5.5V)
- High Bandwidth: -3dB @700MHz
- High Off-Isolation: -100dB at 100KHz
- Low Channel to Channel Crosstalk: 97dB @ 100KHz
- ESD Tolerance: 2kV HBM
- Available in Green SOT23-6 and SOT363 Package

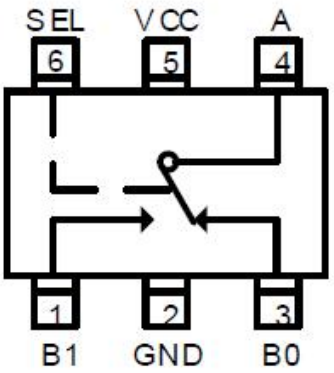
Applications

- Audio, Video, UART, USB2.0 Signal and Supply Routing
- Portable Instrumentation
- Battery-Operated Equipment
- Computer Peripherals
- Cell Phones
- PDAs
- MP3s

Order information

Mode	Package	Specified Temperature range	Ordering Number	Packing Option
FSW3157	SOT23-6	-40℃ to +85℃	FSW3157YSOT236G/TR	Tape and Reel,3000
	SOT363	-40℃ to +85℃	FSW3157YSOT363G/TR	Tape and Reel,3000

Pin Configuration



Pin#	Pin Name	Description
1	B1	Analog/Digital Signal Port (Normally open)
2	GND	Ground
3	B0	Analog/Digital Signal Port (Normally closed)
4	A	Common Signal Port
5	VCC	Single Power Supply
6	SEL	Logic Input Control

Function Table

Logic Input	Function
SEL=0	B0=A
SEL=1	B1=A

Absolute Maximum Ratings(1)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 ~ 6.5	V
Control Input Voltage	V_{SEL}	-0.3 ~ 6.5	V
Continuous Current Through A, B0, B1		±100	mA
Peak Current Through A, B0, B1 (pulsed at 1ms 50% duty cycle)		±200	mA
Storage Temperature Range	T_{STG}	-55 ~ 150	℃
Junction Temperature under Bias	T_J	150	℃
Lead Temperature (Soldering, 10 seconds)	T_L	260	℃
Thermal resistance	$R_{\theta JA}$	350	℃/W

Note:

1. “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.

Recommend operating ratings

Parameter	Symbol	Value	Unit
Supply Voltage Operating	V_{CC}	1.5 ~ 5.5	V
Control Input Voltage	V_{SEL}	-0.3 ~ 5.5 V	V
Input Signal Voltage	V_A	-0.3 ~ 5.5	V
Operating Temperature	T_A	-40 ~ 85	℃

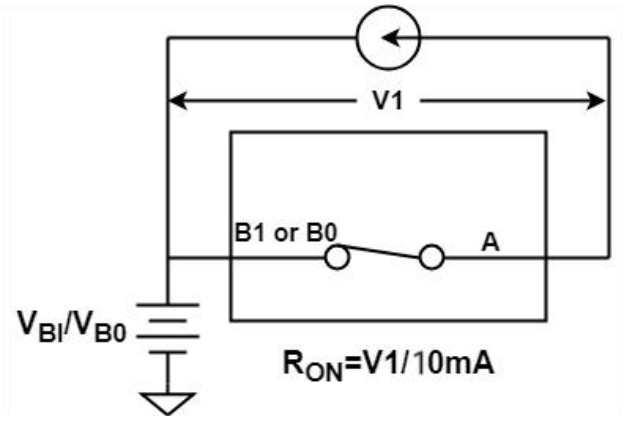
Electrical Characteristics

(T_A=25°C, VCC=3.3V, unless otherwise specified)

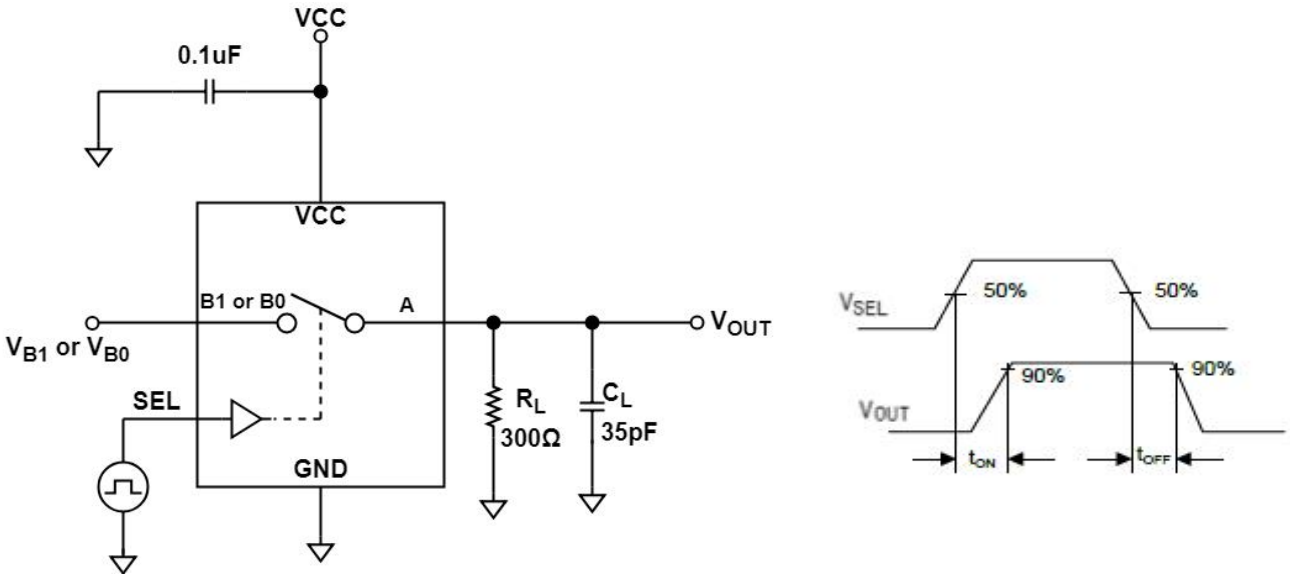
Parameter	Symbol	conditions	Min.	Typ.	Max	Unit
DC CHARACTERISTICS						
Input logic high level	V_{IH}	VCC=3.3~5.5V	1.6			V
		VCC=1.5~3.3V	1.4			V
Input logic low level	V_{IL}	VCC=3.3~5.5V			0.6	V
		VCC=1.5~3.3V			0.4	V
Supply quiescent current	I_{CC}	I_A=0, V_{SEL} =0 or V_{SEL} =VCC			1.0	uA
Increase in I_{CC} per input	I_{CCT}	I_A=0, VCC=4.5V V_{SEL}>1.8 or V_{SEL}<0.5			1.0	uA
Off state leakage from A to B0 (or B1)	I_A	V_A = 5.5V , $V_{B0(or\ B1)}$ = 0V			±3.5	uA
On-Resistance	R_{ON1}	V_A=0 ~ 1.5V,			7.5	Ω
	R_{ON2}	V_A=1.5 ~ 2.0V			3.5	Ω
	R_{ON3}	V_A=2.0 ~ 2.5V			3	Ω
	R_{ON4}	V_A=2.5 ~ 4.0V			2.5	Ω
On-Resistance Flatness	R_{FLAT1}	V_A=0 ~ 0.5V		0.7		Ω
	R_{FLAT2}	V_A=0.5 ~ 2.0V		0.5		Ω
	R_{FLAT3}	V_A=2.0 ~ 4.0V		1.6		Ω
	R_{FLAT4}	V_A=4.0 ~ 5.5V		0.3		Ω
On-Resistance Matching Between Channels	Δ RON	V_A=0~5.5V		0.1	0.2	Ω
AC CHARACTERISTICS						
Turn-On Time	T_{ON}	V_A=1.5V, C_L=35pF, RL=50Ω		200		nS
Turn-Off Time	T_{OFF}	V_A=1.5V, C_L=35pF, R_L=50Ω		200		nS
Break-Before-Make time	T_{BBM}	V_A=1.5V, C_L=35pF, R_L=50Ω		500		nS
-3dB Bandwidth	BW	R_L=50Ω, C_L=0pF		700		MHZ
Off isolation	OIRR	F=1KHz, R_L=50Ω		-81		dB
		F=10KHz, R_L=50Ω		-80		dB

Crosstalk	Xtalk	F=1KHz, R_L=50Ω		-83		dB
		F=10KHz, R_L=50Ω		-82		dB
Total Harmonic Distortion	THD	F=20Hz to 20KHz V_A=600mVp-p @R_L=32Ω,		-80		dB
CAPACITANCE						
Off capacitance	C_{OFF}	F=100KHz, VCC=3.3		5		pF
On capacitance	C_{ON}	F=100KHz, VCC=3.3		7		pF

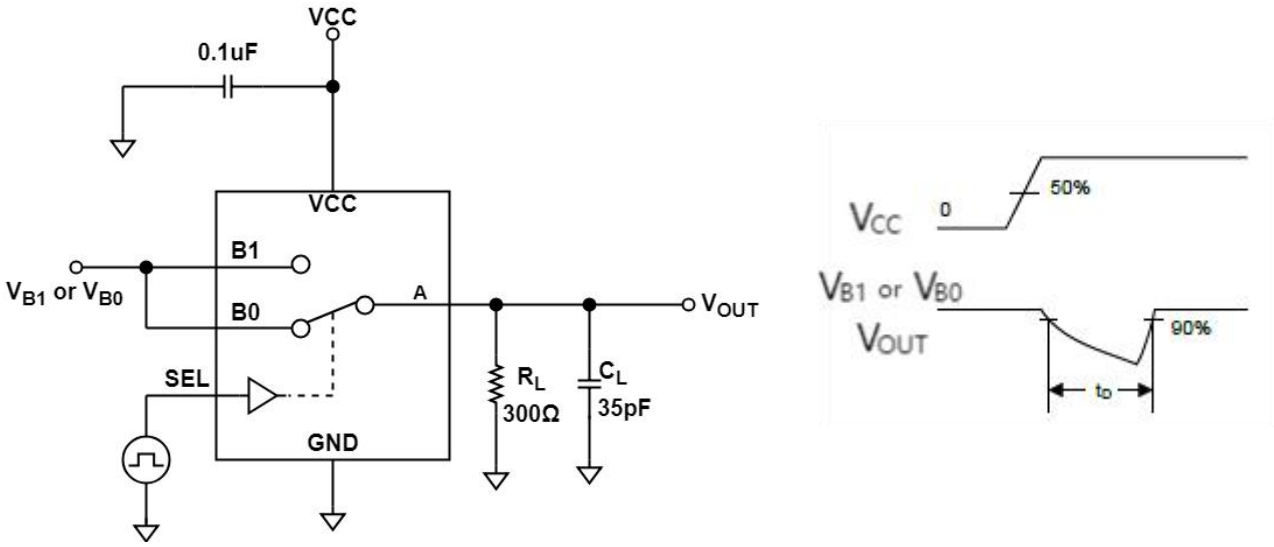
Test Circuits



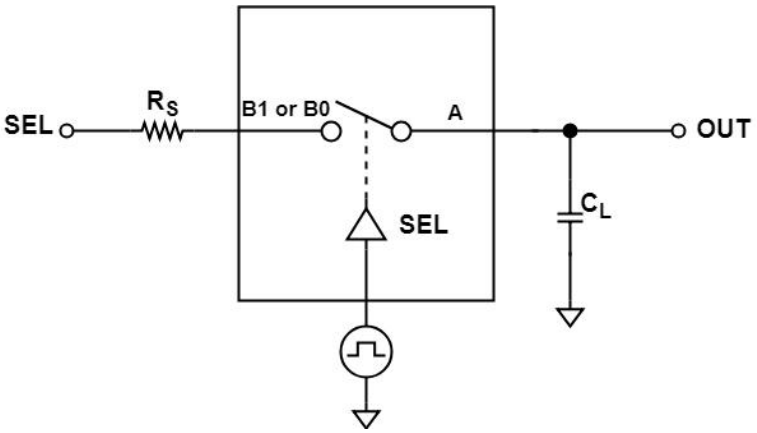
Test Circuit 1. On-Resistance



Test Circuit 2. Switching Times



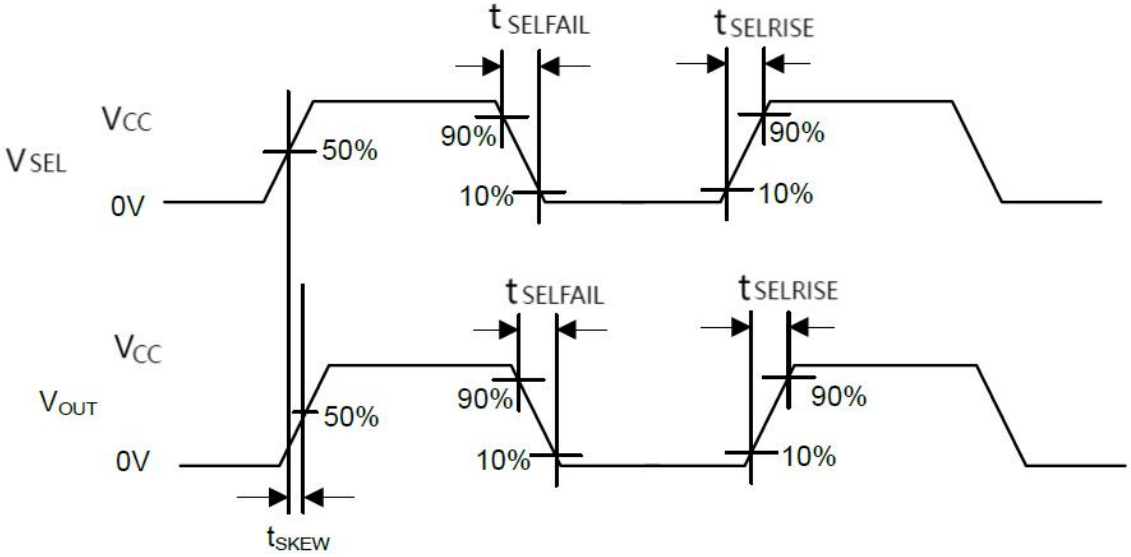
Test Circuit 3. Break-Before-Make Time Delay, t_D



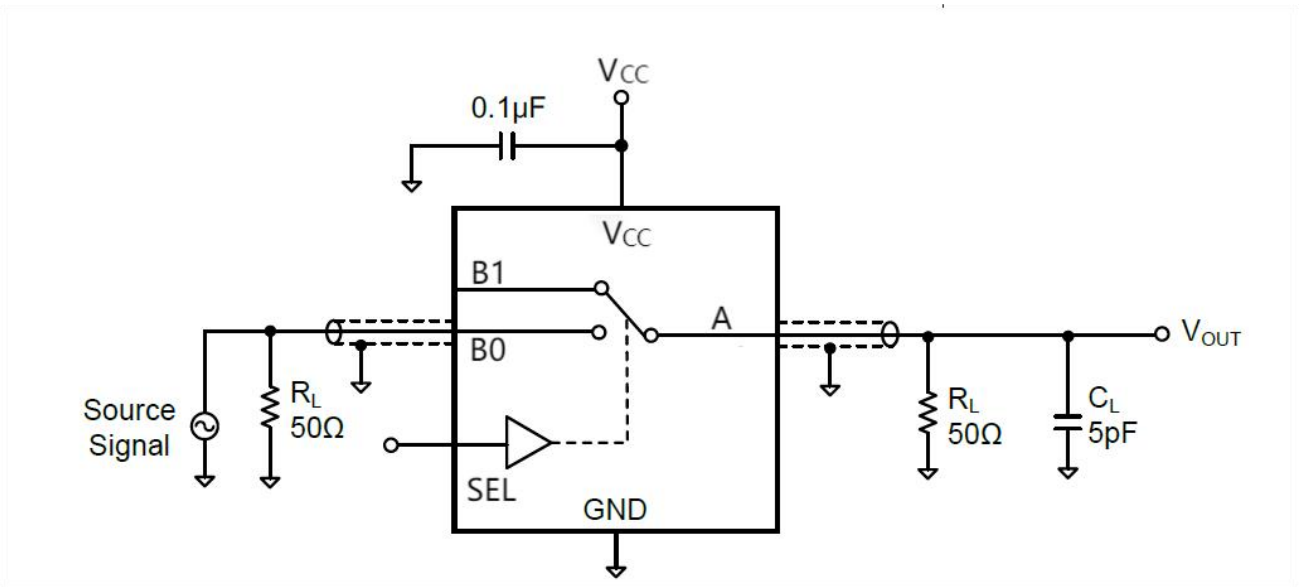
Rise Time Delay = $|t_{SELRISE}-t_{OUTRISE}|$

Fall Time Delay = $|t_{SELFALL}-t_{OUTFALL}|$

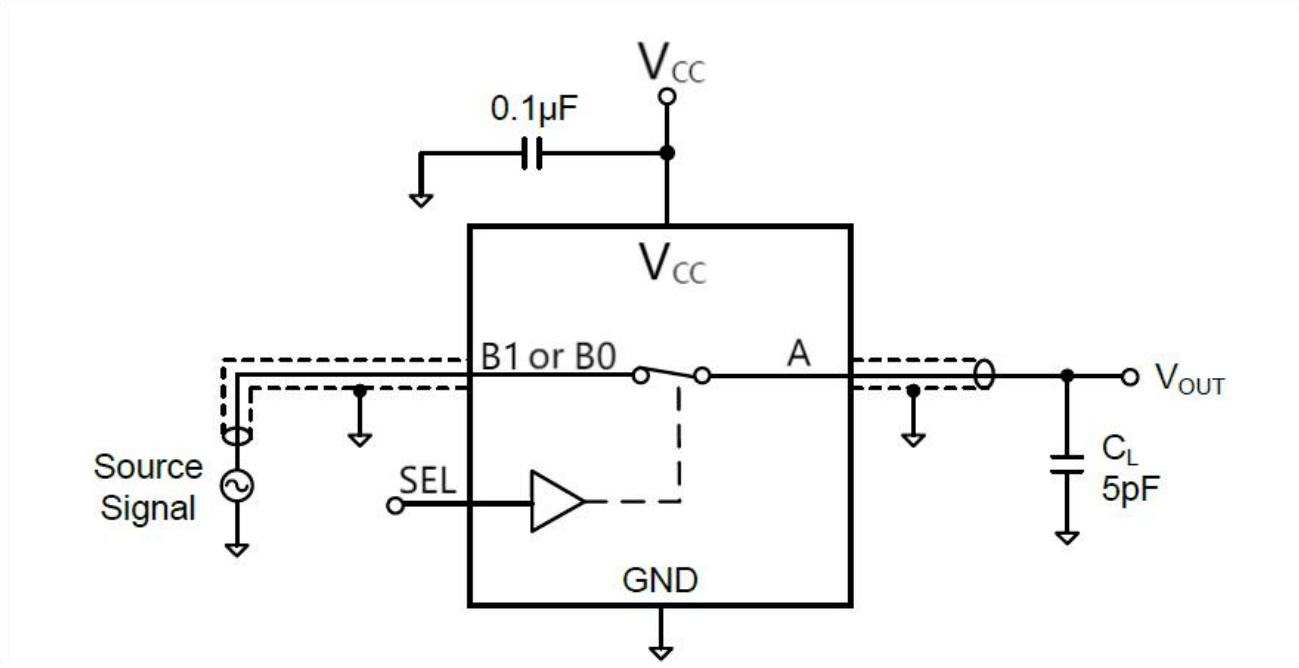
Rise Time to Fall Time Mismatch = $|t_{OUTFALL}-t_{OUTRISE}|$



Test Circuit 4. Output Signal Skew



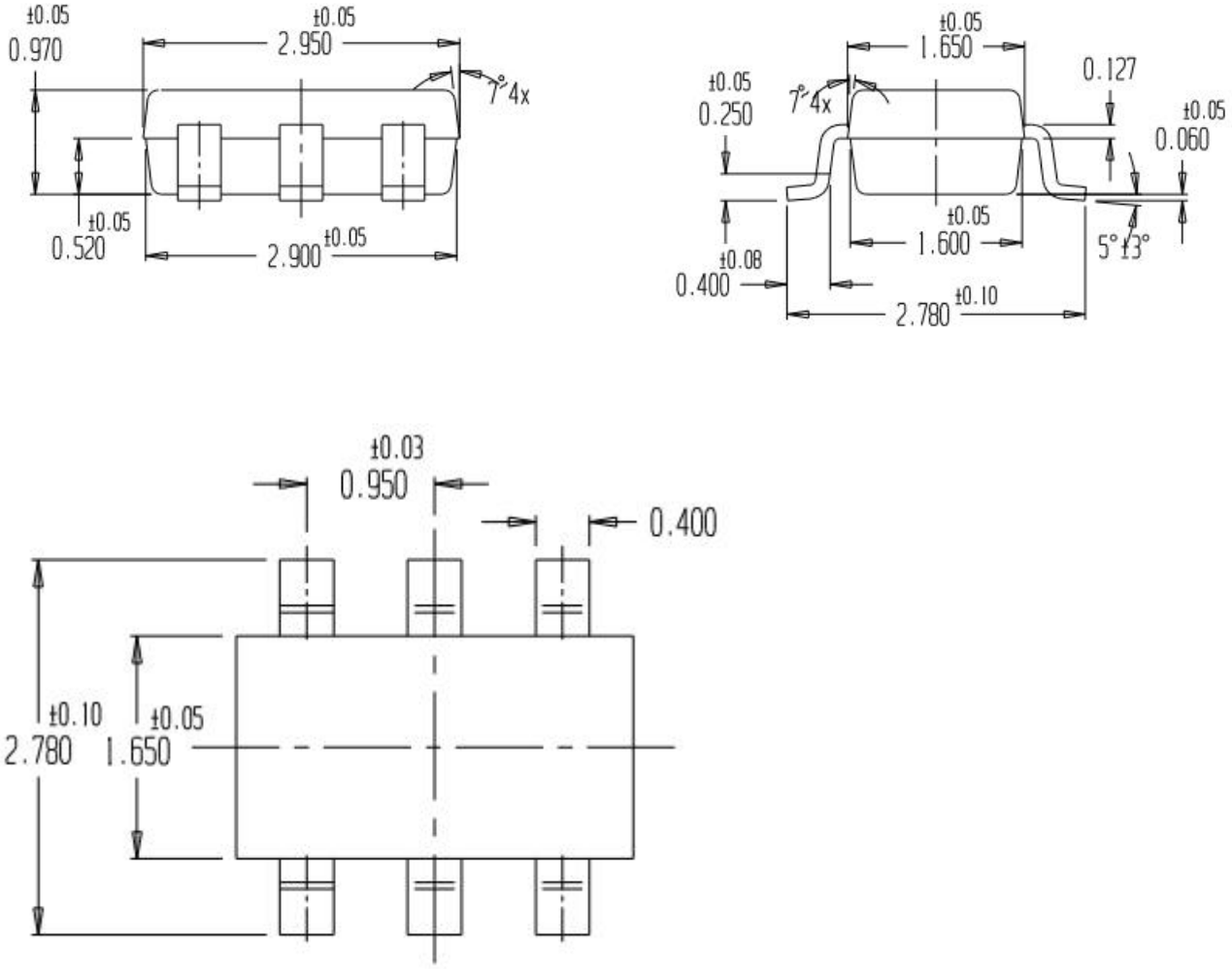
Test Circuit 5. Off Isolation



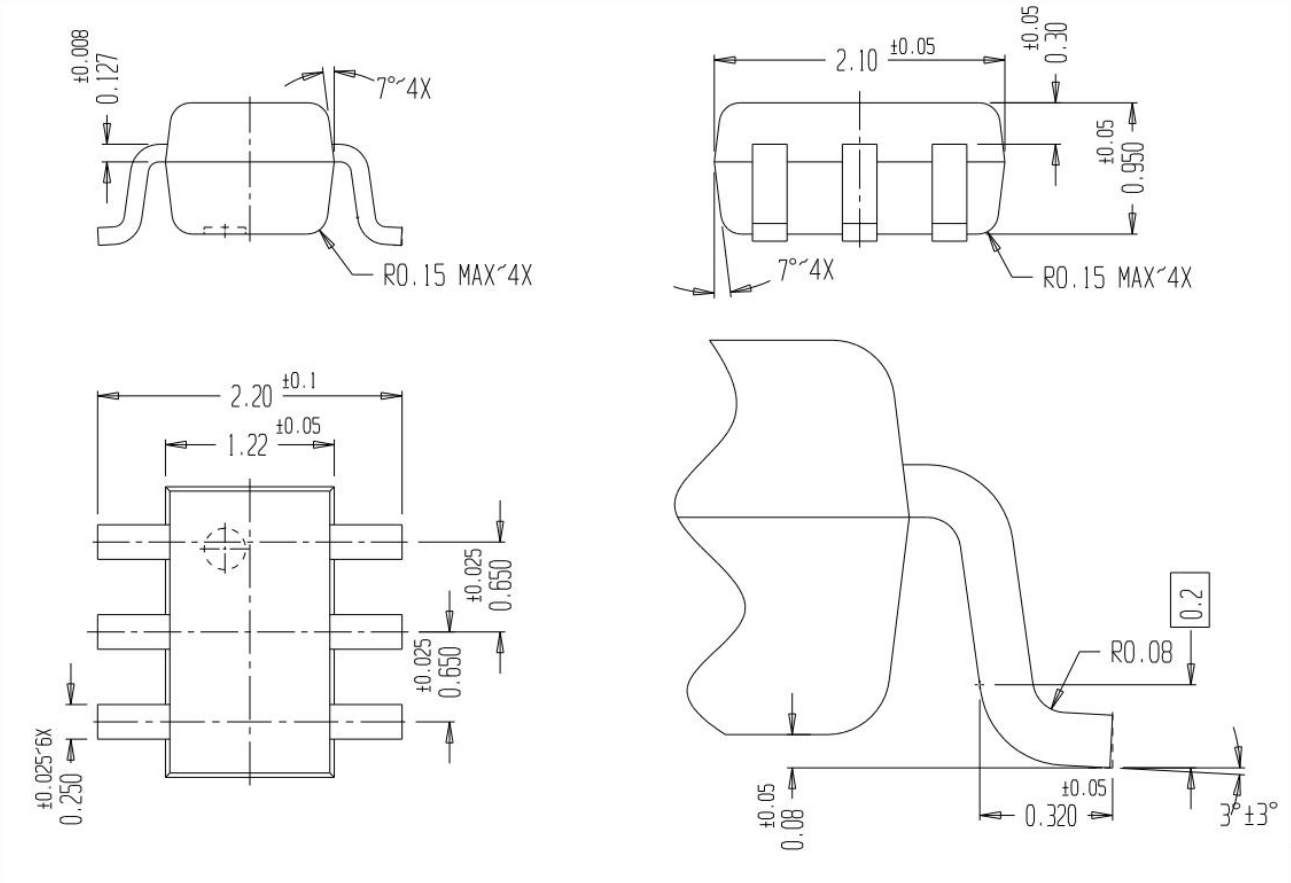
Test Circuit 6. -3dB Bandwidth

Package Outline Dimensions(All dimensions in mm.)

(1) Package Type: SOT23-6



(2) Package Type: SOT363



Version Modification Record

Version Number	Revision	Date
first edition		/
V1.0	1. Update the On-Resistance on page 3 2. Update the Test Circuit 1 on page 4 3. Update the Off state leakage from A to B0(or B1) on page 4	2024/06/20