Three-Channel Differential 4:1 USB 3.1 Super Speed 10Gbps & USB 2.0 Mux/DeMux

Descriptions

The FSW6820 is a high-speed bidirectional passive switch in mux or demux configurations . It suited for USB Type-C™ application supporting switch between four differential signals such as "USB super speed + USB high speed". Based on control pin SEL1 & SEL2, the device provides switching on differential channels between Port A or Port B or Port C to Port COM. The FSW6820 is a generic analog differential passive switch that can work for any high-speed interface applications requiring a common mode voltage range of 0 to 2 V and differential signaling with differential amplitude up to 1800 mVpp. It employs adaptive tracking that ensures the channel remains unchanged for the entire common mode voltage range. Excellent dynamic characteristics of the device allow high-speed switching with minimum attenuation to the signal eye diagram with very little added jitter. It consumes <2mW of power when operational and has a shutdown mode exercisable by EN Pin resulting <20uW.

Features

- Three-Differertial Channel 4:1 Mux/DeMux
- USB 3.1 Super Speed 10Gbps Switch
- USB 3.1 High Bandwidth: 10.87GHz @-3dB BW
- USB 2.0 Bandwidth:1GHz
- Supports both AC coupled and DC coupled signals
- Isolation: -40dB @ 2.0 Gbps
- Crosstalk: -31dB @ 2.0 Gbps
- ESD Tolerance: 2kV HBM
- Low bit-to-bit skew, Bidirectional

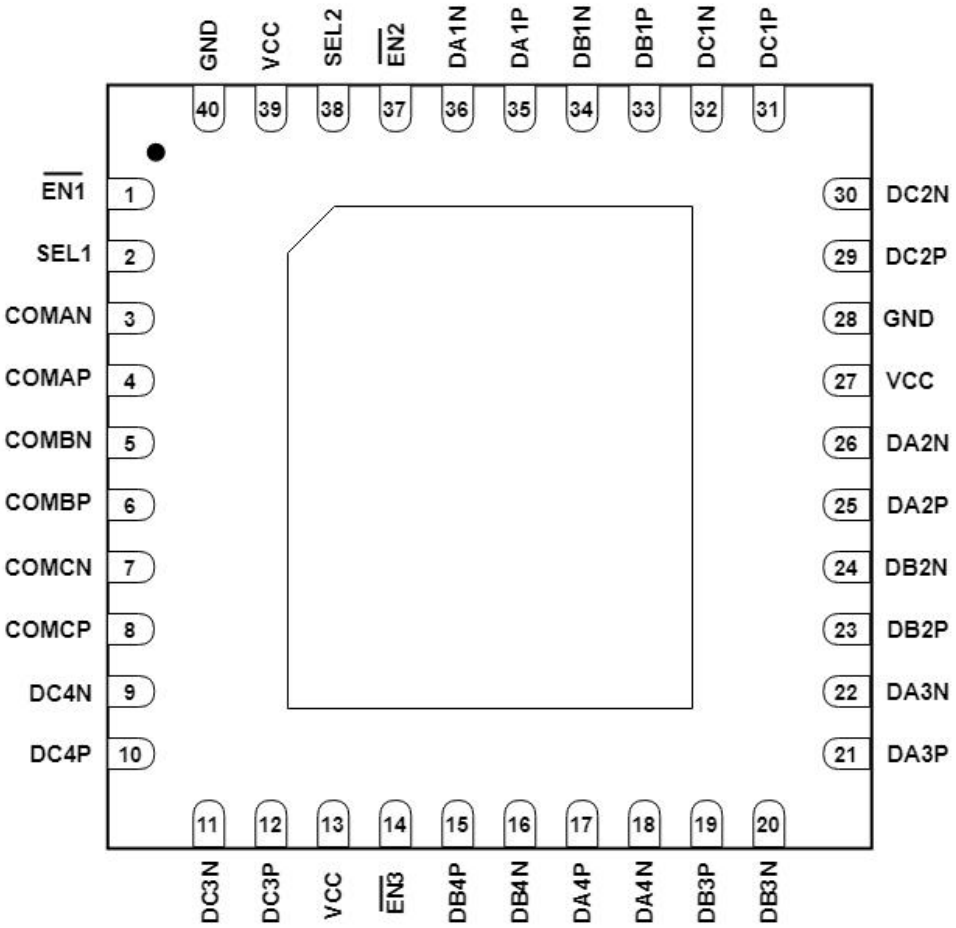
Applications

- USB Type-C Ecosystem
- Desktop and Notebook PCs
- Server/Storage Area Networks
- PCI Express Backplanes
- Shared I/O Ports
- FPD LinkII and FPD LinkIII Switching

Order information

Mode	Package	Specified Temperature range	Ordering Number	Packing Option
FSW6820	QFN5x5-40L	-40℃ to +85℃	FSW6820YQFN40G/TR	Tape and Reel,5000

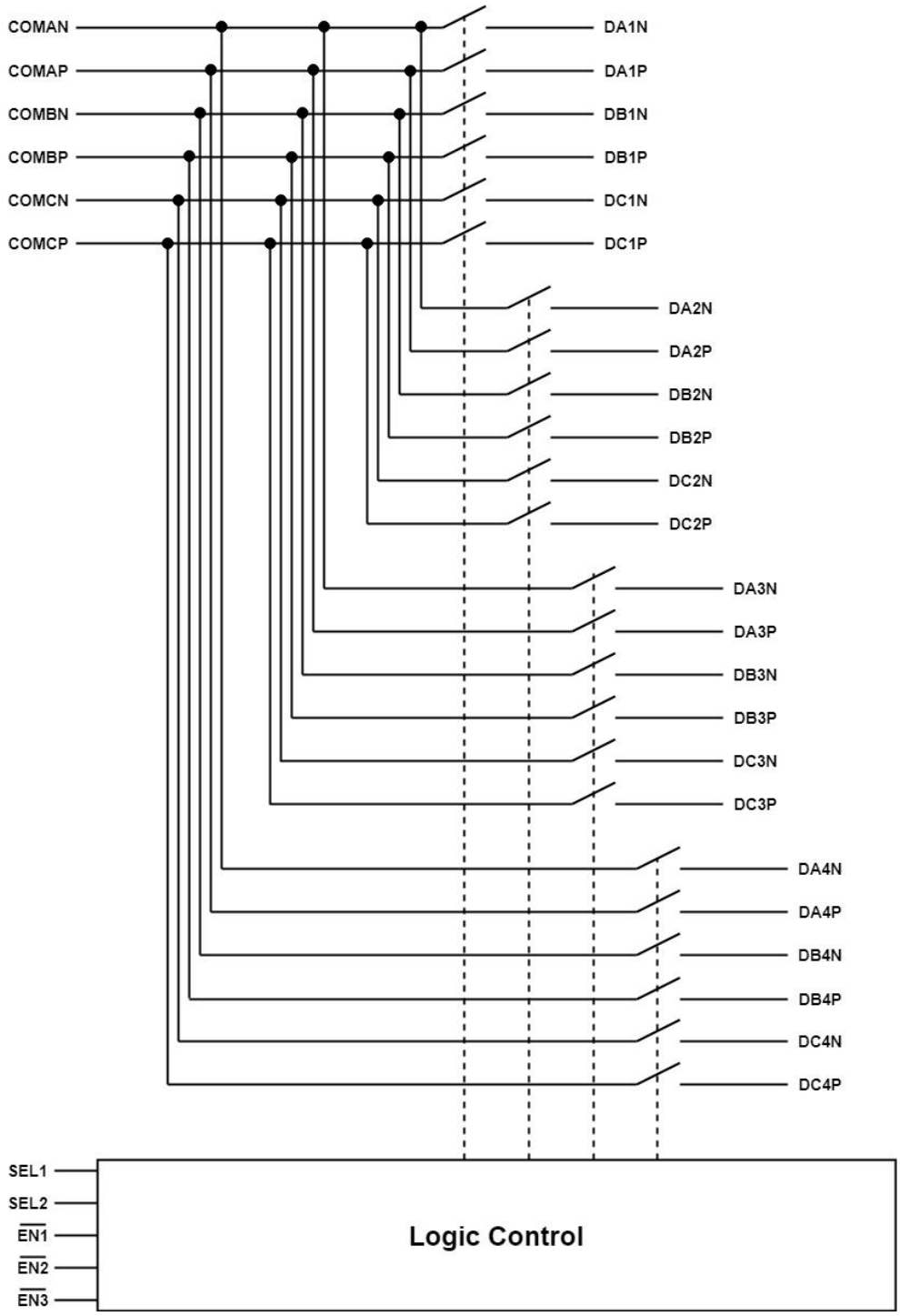
Pin Configuration



Pin#	Pin Name	Signal Type	Description
1	$\overline{EN1}$	I	Enable Pin,Active Low
2	SEL1	I	Select Pin, See Truth Table
3	COMAN	I/O	Negative differential signal 1 for USB 3.1 port COM
4	COMAP	I/O	Positive differential signal 1 for USB 3.1 port COM
5	COMBN	I/O	Negative differential signal 2 for USB 3.1 port COM
6	COMBP	I/O	Positive differential signal 2 for USB 3.1 port COM
7	COMCN	I/O	Negative differential signal 3 for USB 2.0 port COM
8	COMCP	I/O	Positive differential signal 3 for USB 2.0 port COM
9	DC4N	I/O	Negative differential signal 4 for USB 2.0 port C
10	DC4P	I/O	Positive differential signal 4 for USB 2.0 port C
11	DC3N	I/O	Negative differential signal 3 for USB 2.0 port C
12	DC3P	I/O	Positive differential signal 3 for USB 2.0 port C
13	VCC	Power	Positive Supply Voltage

14	$\overline{EN3}$	I	Enable Pin,Active Low
15	DB4P	I/O	Positive differential signal 4 for USB 3.1 port B
16	DB4N	I/O	Negative differential signal 4 for USB 3.1port B
17	DA4P	I/O	Positive differential signal 4 for USB 3.1 port A
18	DA4N	I/O	Negative differential signal 4 for USB 3.1 port A
19	DB3P	I/O	Positive differential signal 3 for USB 3.1 port B
20	DB3N	I/O	Negative differential signal 3 for USB 3.1 port B
21	DA3P	I/O	Positive differential signal 3 for USB 3.1 port A
22	DA3N	I/O	Negative differential signal 3 for USB 3.1 port A
23	DB2P	I/O	Positive differential signal 2 for USB 3.1 port B
24	DB2N	I/O	Negative differential signal 2 for USB 3.1 port B
25	DA2P	I/O	Positive differential signal 2 for USB 3.1 port A
26	DA2N	I/O	Negative differential signal 2 for USB 3.1port A
27	VCC	Power	Positive Supply Voltage
28	GND	Ground	Power Ground
29	DC2P	I/O	Positive differential signal 2 for USB 2.0 port C
30	DC2N	I/O	Negative differential signal 2 for USB 2.0 port C
31	DC1P	I/O	Positive differential signal 1 for USB 2.0 port C
32	DC1N	I/O	Negative differential signal 1 for USB 2.0 port C
33	DB1P	I/O	Positive differential signal 1 for USB 3.1 port B
34	DB1N	I/O	Negative differential signal 1 for USB 3.1 port B
35	DA1P	I/O	Positive differential signal 1 for USB 3.1 port A
36	DA1N	I/O	Negative differential signal 1 for USB 3.1 port A
37	$\overline{EN2}$	I	Enable Pin,Active Low
38	SEL2	I	Select Pin, See Truth Table
39	VCC	Power	Positive Supply Voltage
40	GND	Ground	Power Ground

Block Diagram



Truth Table

$\overline{EN1}$ & $\overline{EN2}$ & $\overline{EN3}$	SEL1	SEL2	Channel
High	X	X	X
Low	Low	Low	1
		High	2
	High	High	3
		Low	4

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Junction Temperature	125°C
Supply Voltage to Ground Potential	-0.5V to +5.5V
Supe Speed Data Channel TX / RX	-0.5V to 3.8V
DC Input Voltage	-0.5V to VCC
DC Output Current	50mA
Power Dissipation	300mW

Notes:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

(TA=25°C, VCC=1.8V, unless otherwise specified)

Parameter	Symbol	conditions	Min.	Typ.	Max.	Unit
POWER SUPPLY						
VCC Quiescent Current	I_Q	SEL=0 or VCC, $\overline{EN1}$ & $\overline{EN2}$ & $\overline{EN3}$ =0		100		uA
Power-down Current	I_{PO}	SEL=0 or VCC, $\overline{EN1}$ & $\overline{EN2}$ & $\overline{EN3}$ =VCC			3	uA
DC CHARACTERISTICS						
Input logic high	V_{IH}	VCC=1.8~4.5V	1.6			V
Input logic low	V_{IL}	VCC=1.8~4.5V			0.4	V
$\overline{EN}$ Internal pull-up resistor	R_{UP}			2		MΩ
SEL Internal pull-down resistor	R_{DN}			2		MΩ
On-Resistancefor TX/RX	R_{ON_HS}	V_{IS}= 0.2V I_{ON}=8mA		13.4		Ω
R_{ON} Flatness for TX/RX	R_{FLAT_LP}	V_{IS}= 0 to 1.2V I_{ON}=8mA		0.8	1	Ω
R_{ON} Flatness for TX/RX	R_{FLAT_LP}	V_{IS}= 0 to 0.2V I_{ON}=8mA		0.2	0.3	Ω
R_{ON} Matching Between Channels	R_{MATCH}	V_{IS}= 0 to 1.2V I_{ON}=8mA		0.1		Ω
AC CHARACTERISTICS						
Enable Time $\overline{EN}$ to Output	t_{EN}	R_L=50Ω C_L=0pF V_{IS}= 0.6V		80	150	uS
Disable Time $\overline{EN}$ to Output	t_{DIS}	R_L=50Ω C_L=0pF V_{IS}= 0.6V		40	250	nS
Turn-On Time SEL to Output	t_{ON}	R_L=50Ω C_L=0pF V_{IS}= 0.6V		400	1200	nS
Turn-Off Time SEL to Output	t_{OFF}	R_L=50Ω C_L=0pF V_{IS}= 0.6V		130	800	nS
Break-Before-Make Time	t_{BBM}	R_L=50Ω C_L=0pF V_{IS}= 0.6V		250	800	nS
Propagation Delay	t_{PD}	R_L=50Ω C_L=0pF V_{IS}= 0.6V		0.25		nS
Off Isolation	Off	R_L = 50Ω f = 1.2GHz V_{IS}= 0.2V_{PP}, See Fig.2		-27		dB
Crosstalk	X_{TALK}	R_L = 50Ω f = 1.2GHz V_{IS}= 0.2V_{PP}, See Fig.1		-43		dB

-3dB Bandwidth	BW_{-3dB}	R_L=50Ω C_L=0pF Signal 0dBm		10.87		GHz
CAPACITANCE						
Switch On Capacitance	C_{ON}	V_{Bias} = 0.2V, f = 1.5GHz		1.5		pF
Switch Off Capacitance	C_{OFF}	V_{Bias} = 0.2V, f = 1.5GHz		1.0		pF

Notes:

(1) Flatness is defined as the difference between maximum and minimum value of ON-resistance at the specified analog signal voltage points.

(2) R_{ON} matching between channels is calculated by subtracting the channel with the lowest max Ron value from the channel with the highest max Ron value.

(3) Crosstalk is inversely proportional to source impedance

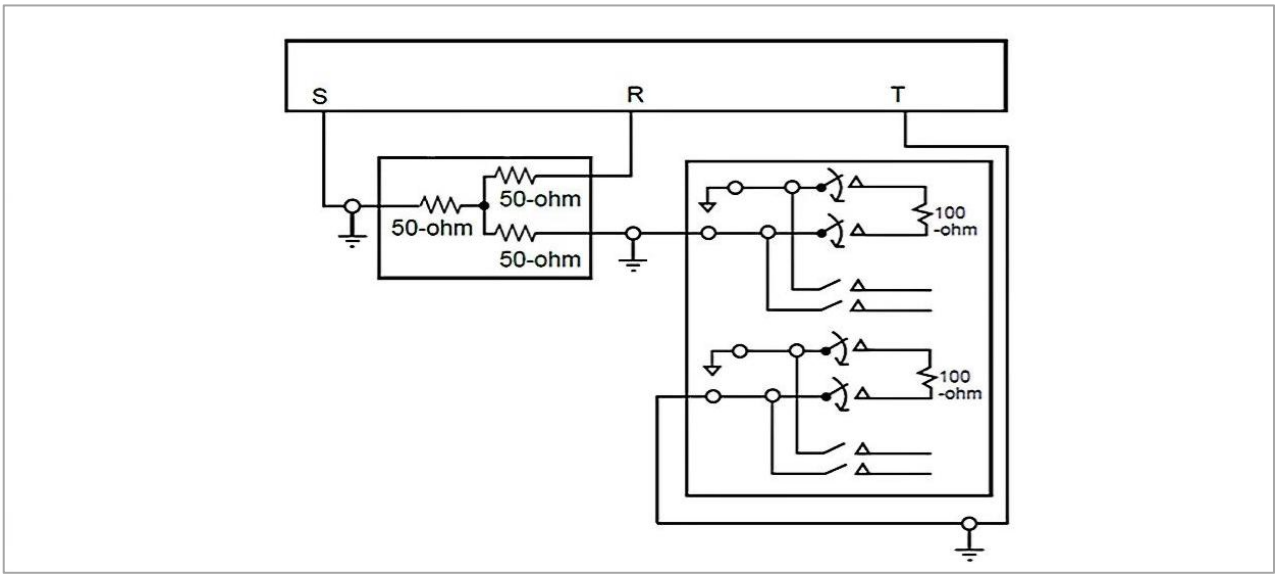


Fig.1 Crosstalk Setup

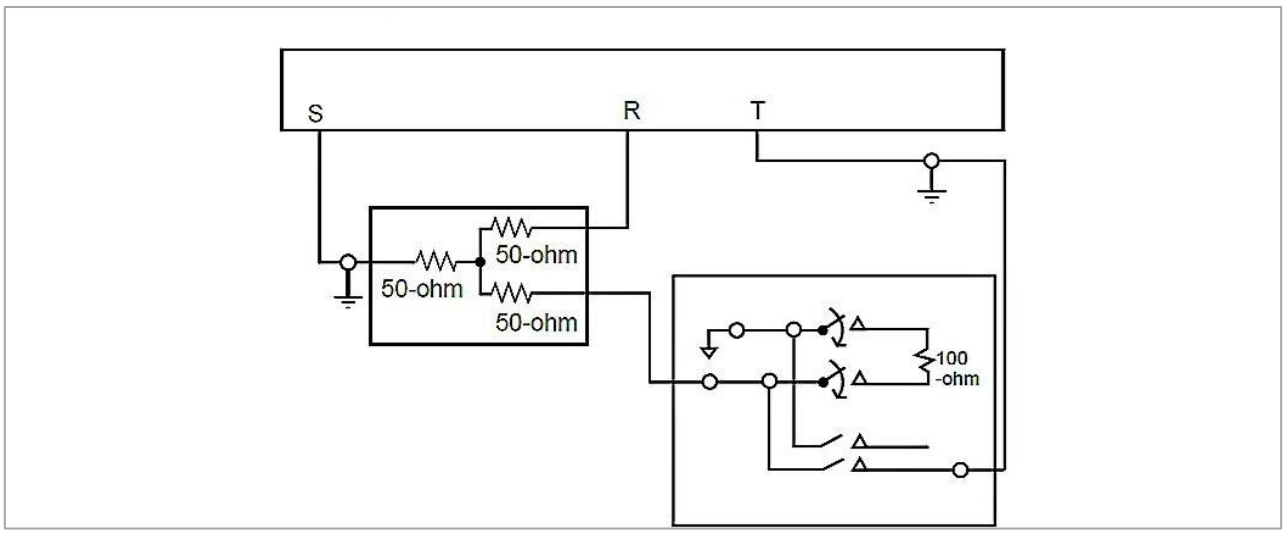


Fig.2 OFF-isolation

Application Information

Many interfaces require AC coupling between the transmitter and receiver. The 0402 capacitors are the preferred option to provide AC coupling, and the 0603 size capacitors also work. The 0805 size capacitors and C-packs should be avoided. When placing AC coupling capacitors symmetric placement is best. A capacitor value of 0.1 μF is best and the value should be match for the ± signal pair. The placement should be along the TX pairs on the system board, which are usually routed on the top layer of the board.

There are several placement options for the AC coupling capacitors. Because the switch requires a bias voltage, the capacitors must only be placed on one side of the switch. If they are placed on both sides of the switch, a biasing voltage should be provided. A few placement options are shown below. In Figure 1, the coupling capacitors are placed between the switch and endpoint. In this situation, the switch is biased by the system/host controller.

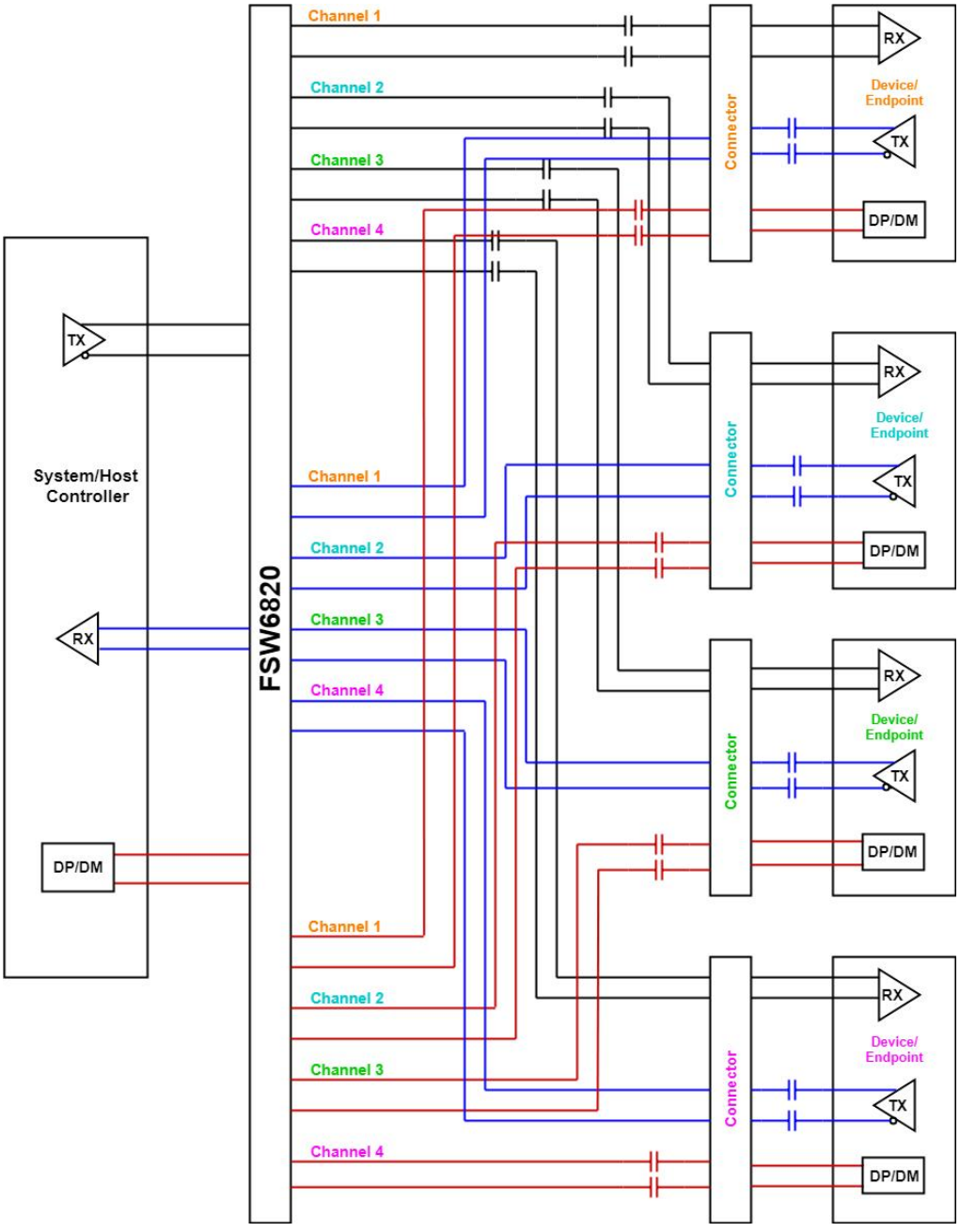


Figure 1. AC Coupling Capacitors Between Switch Tx and Endpoint Tx

In Figure 2, the coupling capacitors are placed on the host transmit pair and endpoint transmit pair. In this situation, the switch on the top is biased by the endpoint and the lower switch is biased by the host controller.

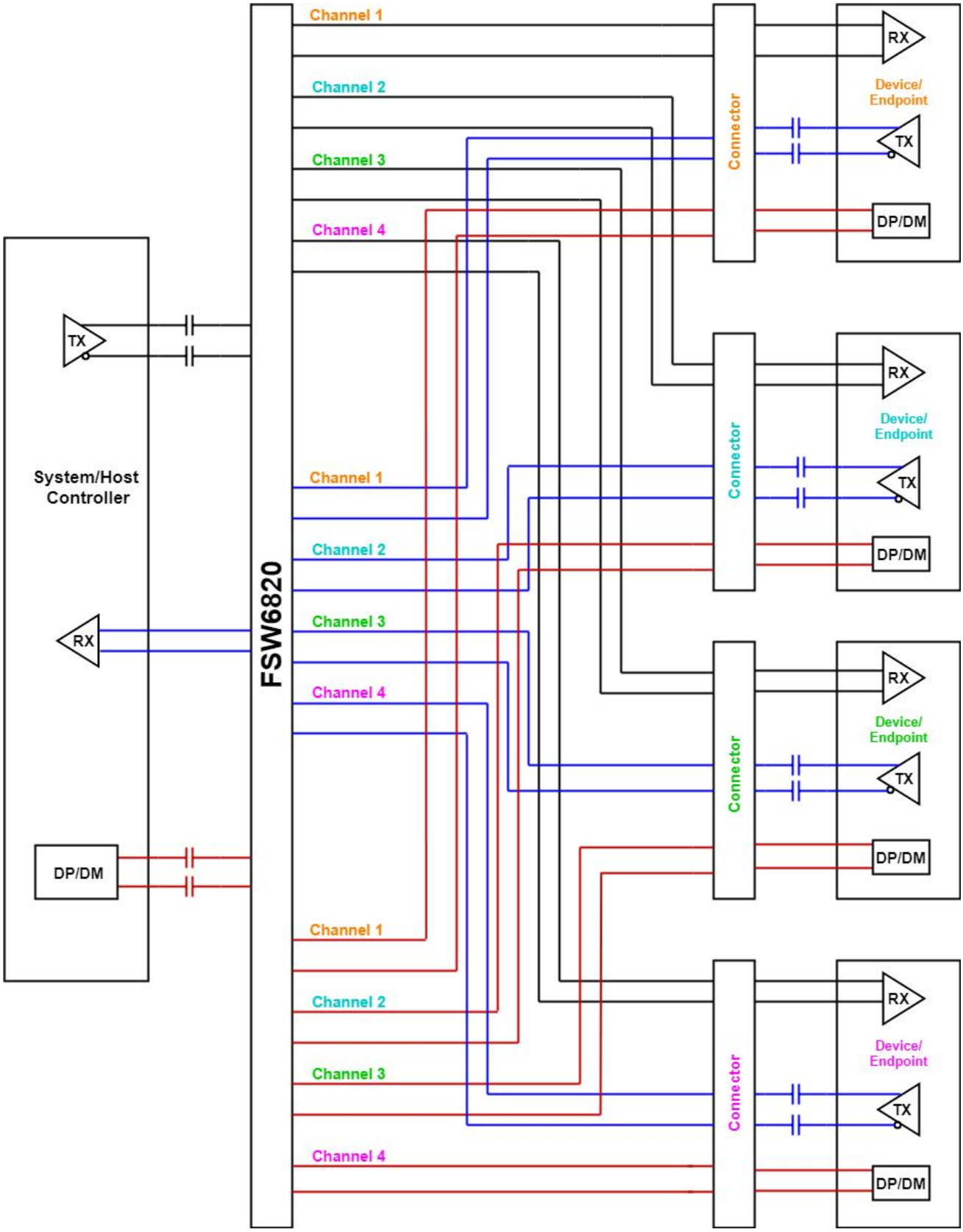


Figure 2. AC Coupling Capacitors on Host Tx and Endpoint Tx

If the common-mode voltage in the system is higher than 2V, the coupling capacitors are placed on both sides of the switch (shown in Figure 3). A biasing voltage of less than 2V is required in this case.

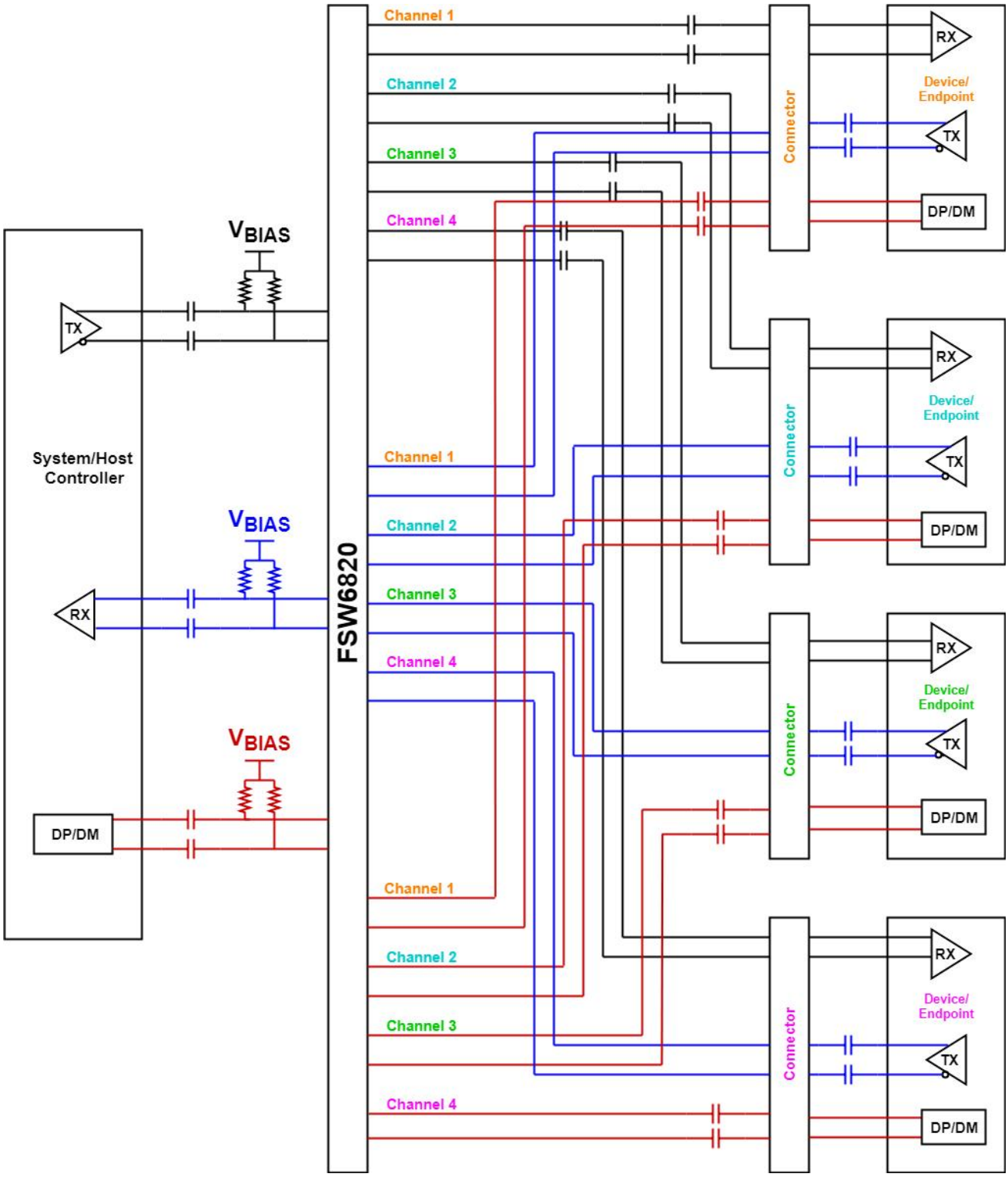
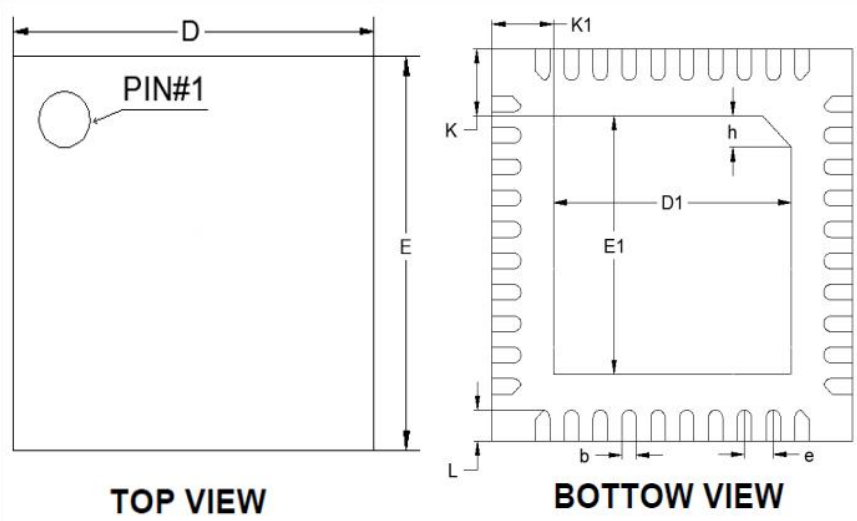


Figure 3. AC Coupling Capacitors on Both Sides of Switch

Package Outline Dimensions(All dimensions in mm.)

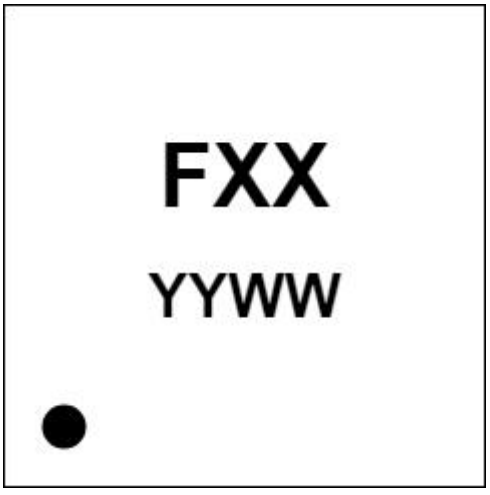
(1) Package Type: QFN5x5-40L



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1		0.203BSC	
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D1	3.20	3.30	3.40
E1	3.20	3.30	3.40
b	0.15	0.20	0.25
e		0.4BSC	
L	0.35	0.40	0.45
K	0.80	0.85	0.90
K1	0.80	0.85	0.90
h	0.35	0.40	0.45

(2) Top Marking Information

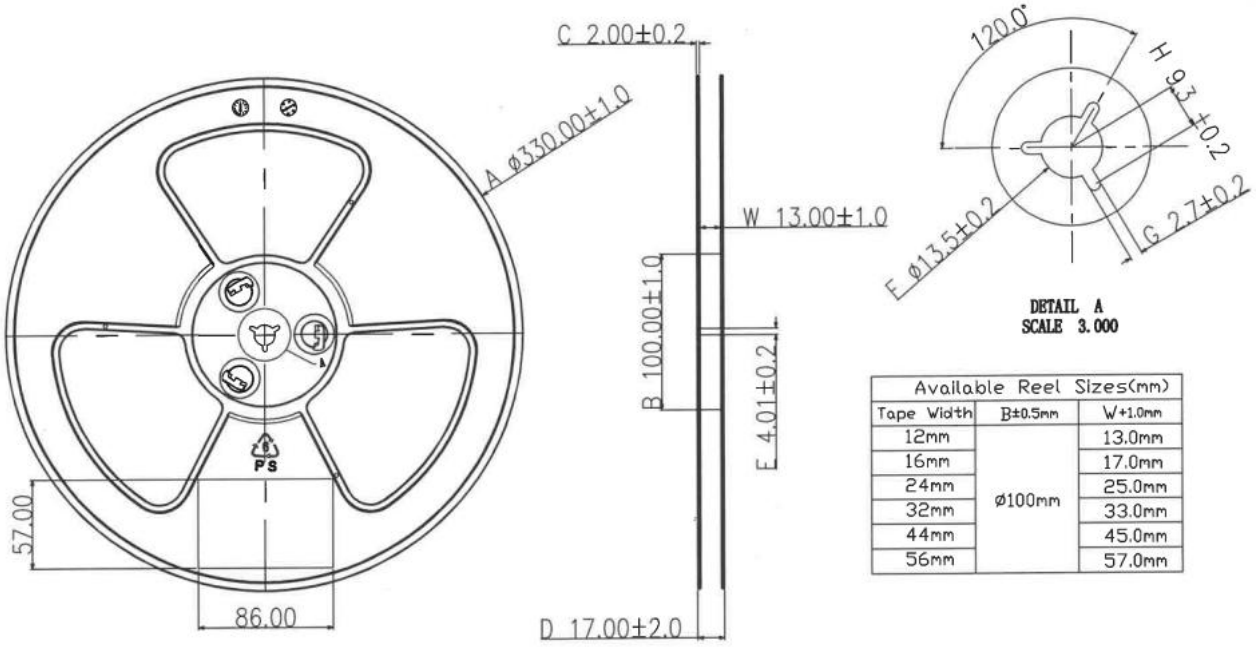


YY: Year (23=2023,24=2024…)

WW: Weekly (01-53)

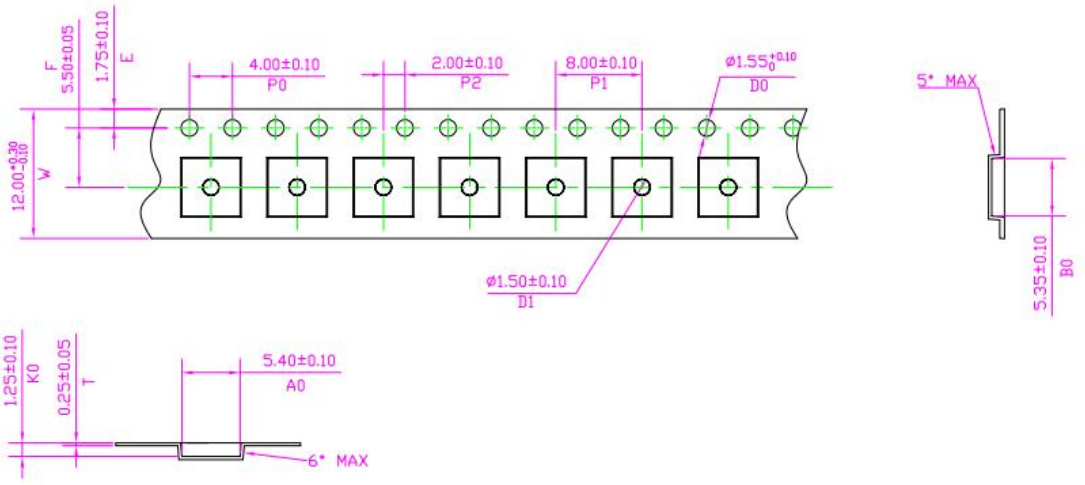
AXX: Imternal ID Code

TAPE AND REEL INFORMATION



Available Reel Sizes(mm)		
Tape Width	B±0.5mm	W+1.0mm
12mm	ø100mm	13.0mm
16mm		17.0mm
24mm		25.0mm
32mm		33.0mm
44mm		45.0mm
56mm		57.0mm

注：1.材质:HIPS
2.单位:mm



NOTE ：
1. 所有尺寸依国际EIA-481-3标准.
2. 任意10个棘轮孔的累积误差不超过 ±0.2mm.
3. 载带长度方向100mm距离的非平行度不可超过1mm.