Five-Channel Differential 2:1 USB 3.1 Super Speed 10Gbps & Two Normal Speed Signal Mux/DeMux

Descriptions

The FSW6860 is a high-speed and normal-speed bidirectional passive switch in mux or demux configurations.

The FSW6860 suited for suited for USB Type-C™ application supporting USB 3.1 Gen 1 and Gen 2 data rates.Based on control pin SEL, the device provides switching on differential channels between Port A or Port B to Port COM. The FSW6860 is a generic analog differential passive switch that can work for any high-speed interface applications requiring a common mode voltage range of 0 to 2 V and differential signaling with differential amplitude up to 1800 mVpp. It employs adaptive tracking that ensures the channel remains unchanged for the entire common mode voltage range. Excellent dynamic characteristics of the device allow high-speed switching with mini-mum attenuation to the signal eye diagram with very little added jitter. It consumes <2mW of power when operational and has a shutdown mode exercisable by EN Pin resulting <20uW.

The FSW6860 normal speed signal is a single, bidirectional, single-pole/ double-throw (SPDT) CMOS analog switch.It target applications for audio switching.It features guaranteed on-resist-ance matching between switches and guaranteed on-resistance flatness over the signal range. This ensures excellent linearity and low distortion when switching audio signals.

Features

High Speed Channel :

- Five-Differertial Channel 2:1 Mux/DeMux
- USB 3.1 Super Speed 10Gbps Switch
- USB 3.1 High Bandwidth: 10.87GHz @-3dB BW
- Supports both AC coupled and DC coupled signals
- Isolation: -40dB @ 2.0 Gbps
- Crosstalk: -31dB @ 2.0 Gbps
- ESD Tolerance: 2kV HBM
- Low bit-to-bit skew, Bidirectional

Normal Speed Signal:

- High Bandwidth: -3dB @700MHz
- High Off-Isolation: -100dB at 100KHz
- Low Channel to Channel Crosstalk: 97dB @100KHz

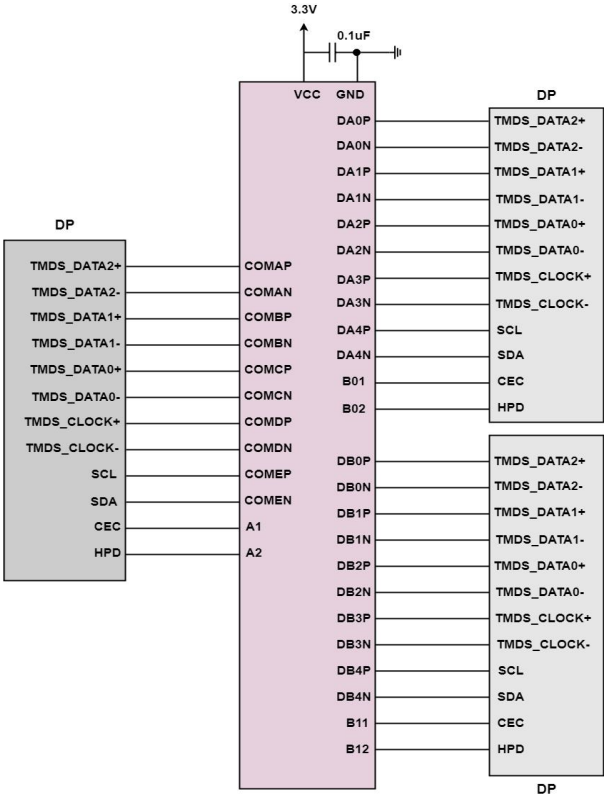
Applications

- USB Type-C Ecosystem
- Desktop and Notebook PCs
- Server/Storage Area Networks
- PCI Express Backplanes
- Shared I/O Ports
- FPD LinkII and FPD LinkIII Switching

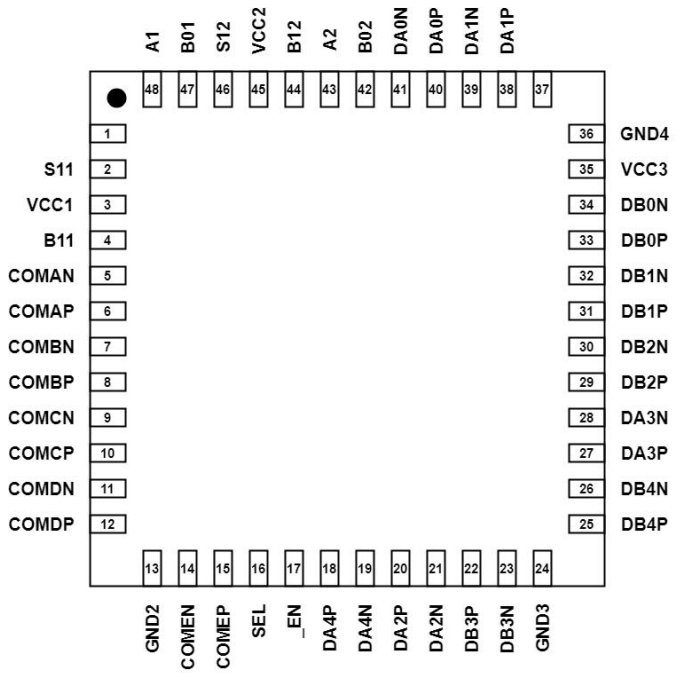
Order information

Mode	Package	Specified Temperature range	Ordering Number	Packing Option
FSW6860	QFN6x6-48L	-40℃ to +85℃	FSW6860YQFN48G/TR	Tape and Reel,3000

Application Information



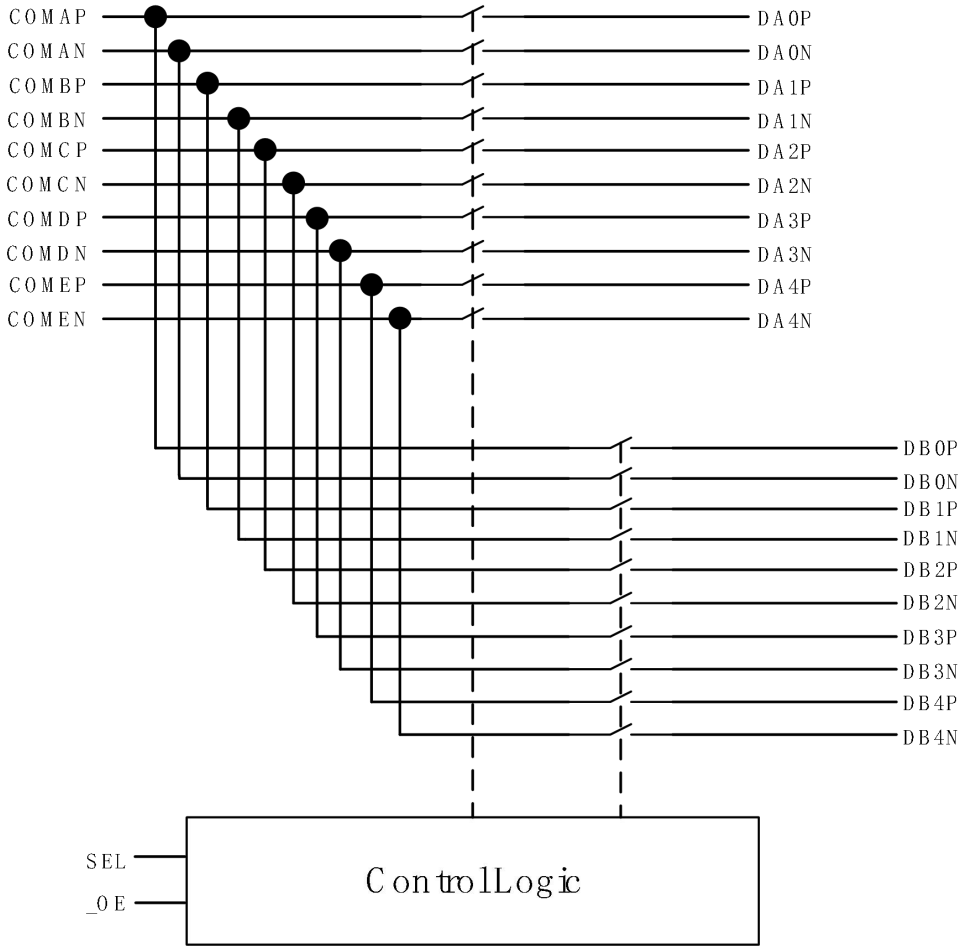
Pin Configuration

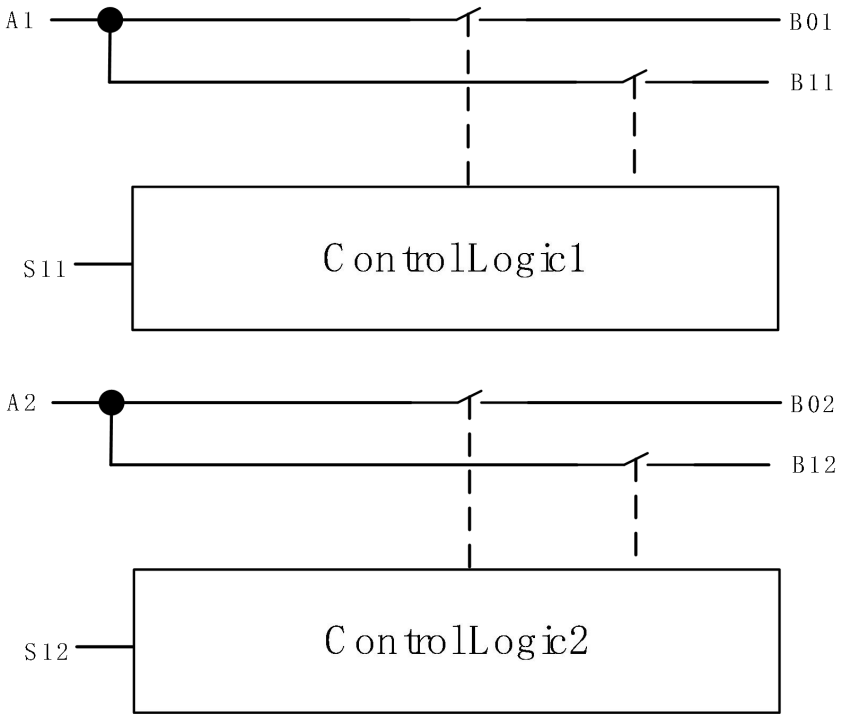


Pin#	Pin Name	Signal Type	Description
1	NC	/	Not Connected
2	S11	I	Select Pin, See Truth Table L:Port A1 to B01 H:Port A1 to B11
3	VCC2	Power	Positive Supply Voltage
4	B11	I/O	Analog/Digital Signal Port1 (Normally open)
5	COMAN	I/O	Negative differential signal 1 for USB 3.1 port COM
6	COMAP	I/O	Positive differential signal 1 for USB 3.1 port COM
7	COMBN	I/O	Negative differential signal 2 for USB 3.1 port COM
8	COMBP	I/O	Positive differential signal 2 for USB 3.1 port COM
9	COMCN	I/O	Negative differential signal 3 for USB 3.1 port COM
10	COMCP	I/O	Positive differential signal 3 for USB 3.1 port COM
11	COMDN	I/O	Negative differential signal 4 for USB 3.1 port COM
12	COMDP	I/O	Positive differential signal 4 for USB 3.1 port COM
13	GND2	Ground	Power Ground
14	COMEN	I/O	Negative differential signal 5 for USB 3.1 port COM
15	COMEP	I/O	Positive differential signal 5 for USB 3.1 port COM
16	SEL	I	Select Pin, See Truth Table. L:Port COM to Port A H:Port COM toPort B
17	_EN	I	Enable Pin, Active Low
18	DA4P	I/O	Positive differential signal 4 for USB 3.1 port A
19	DA4N	I/O	Negative differential signal 4 for USB 3.1 port A
20	DA2P	I/O	Positive differential signal 2 for USB 3.1 port A
21	DA2N	I/O	Negative differential signal 2 for USB 3.1port A
22	DB3P	I/O	Positive differential signal 3 for USB 3.1 port B
23	DB3N	I/O	Negative differential signal 3 for USB 3.1 port B
24	GND3	Ground	Power Ground
25	DB4P	I/O	Positive differential signal 4 for USB 3.1 port B
26	DB4N	I/O	Negative differential signal 4 for USB 3.1 port B
27	DA3P	I/O	Positive differential signal 3 for USB 3.1 port A
28	DA3N	I/O	Negative differential signal 3 for USB 3.1port A
29	DB2P	I/O	Positive differential signal 2 for USB 3.1 port B
30	DB2N	I/O	Negative differential signal 2 for USB 3.1 port B
31	DB1P	I/O	Positive differential signal 1 for USB 3.1 port B
32	DB1N	I/O	Negative differential signal 1 for USB 3.1 port B
33	DB0P	I/O	Positive differential signal 0 for USB 3.1 port B
34	DB0N	I/O	Negative differential signal 0 for USB 3.1 port B
35	VCC3	Power	Positive Supply Voltage
36	GND4	Ground	Power Ground
37	NC	/	Not Connected
38	DA1P	I/O	Positive differential signal 1 for USB 3.1 port A
39	DA1N	I/O	Negative differential signal 1 for USB 3.1 port A

40	DA0P	I/O	Positive differential signal 0 for USB 3.1 port A
41	DA0N	I/O	Negative differential signal 0 for USB 3.1 port A
42	B02	I/O	Analog/Digital Signal Port2 (Normally closed)
43	A2	I/O	Common Signal Port2
44	B12	I/O	Analog/Digital Signal Port2 (Normally open)
45	VCC2	Power	Positive Supply Voltage
46	S12	I	Select Pin, See Truth Table L:Port A2 to B02 H:Port A2 to B12
47	B01	I/O	Analog/Digital Signal Port1 (Normally closed)
48	A1	I/O	Common Signal Port1

Block Diagram





Truth Table

_OE	SEL	Channel
High	X	X
Low	Low	A
	High	B
_OE	S11	Channel
High	X	X
Low	Low	B01
	High	B11
_OE	S12	Channel
High	X	X
Low	Low	B02
	High	B12

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55℃ to +150℃
Junction Temperature	125℃
High Speed Channel	
Supply Voltage to Ground Potential,VCC3	-0.5V to +5.5V
Super Speed Data Channel TX / RX	-0.5V to 3.8V
DC Input Voltage	-0.5V to VCC3
DC Output Current	50mA

Power Dissipation	300mW
Normal Speed Channel	
Supply Voltage,VCC1,VCC2	-0.3~6.5V
Control Input Voltage	-0.3 ~ 6.5V
Continuous Current Through A1, B01, B11	±100mA
Continuous Current Through A2, B02, B12	±100mA
Peak Current Through A1, B01, B11 (pulsed at 1ms 50% duty cycle)	±200mA
Peak Current Through A1, B01, B11 (pulsed at 1ms 50% duty cycle)	±200mA
Thermal resistance	350°C/W

Notes:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

(High speed channel,TA=25°C, VCC(VCC3)=3V, unless otherwise specified)

Parameter	Symbol	conditions	Min.	Typ.	Max.	Unit
POWER SUPPLY (High Speed Channel)						
VCC Quiescent Current	I_Q	SEL=0 or VCC, _EN=0		28		uA
Power-down Current	I_{PO}	SEL=0 or VCC, _EN=VCC			1	uA
DC CHARACTERISTICS (High Speed Channel)						
Input logic high	V_{IH}	VCC=1.8~4.5V	1.6			V
Input logic low	V_{IL}	VCC=1.8~4.5V			0.4	V
$\overline{EN}$ Internal pull-up resistor	R_{UP}			2		MΩ
SEL Internal pull-down resistor	R_{DN}			2		MΩ
On-Resistance for TX/RX	R_{ON_HS}	V_{IS}= 1.5V I_{ON}=8mA		6.5	9.5	Ω
		V_{IS}= 3V I_{ON}=8mA		8.2	11.5	
R_{ON} Matching Between Channels	R_{MATCH}	V_{IS}= 0 to 1.2V I_{ON}=8mA		0.1		Ω
AC CHARACTERISTICS (High Speed Channel)						
Enable Time $\overline{EN}$ to Output	t_{EN}	R_L=50Ω C_L=0pF V_{IS}= 0.6V		80	150	uS
Disable Time $\overline{EN}$ to Output	t_{DIS}	R_L=50Ω C_L=0pF V_{IS}= 0.6V		40	250	nS
Turn-On Time SEL to Output	t_{ON}	R_L=50Ω C_L=0pF V_{IS}= 0.6V		400	1200	nS
Turn-Off Time SEL to Output	t_{OFF}	R_L=50Ω C_L=0pF V_{IS}= 0.6V		130	800	nS
Break-Before-Make Time	t_{BBM}	R_L=50Ω C_L=0pF V_{IS}= 0.6V		250	500	nS
Propagation Delay	t_{PD}	R_L=50Ω C_L=0pF V_{IS}= 0.6V		0.25		nS
Off Isolation	Off	R_L = 50Ω f = 1.2GHz V_{IS}= 0.2V_{PP}, See Fig.2		-27		dB
Crosstalk	X_{TALK}	R_L = 50Ω f = 1.2GHz V_{IS}= 0.2V_{PP}, See Fig.1		-43		dB
-3dB Bandwidth	BW_{-3dB}	R_L=50Ω C_L=0pF Signal 0dBm		10.87		GHz

CAPACITANCE (High Speed Channel)						
Switch On Capacitance	C_{ON}	V_{Bias} = 0.2V, f = 1.5GHz		1.5		pF
Switch Off Capacitance	C_{OFF}	V_{Bias} = 0.2V, f = 1.5GHz		1.0		pF

(Normal Speed Channel,T_A=25°C, VCC(VCC1,2)=3.3V, unless otherwise specified)

Parameter	Symbol	conditions	Min.	Typ.	Max	Unit
DC CHARACTERISTICS (Normal Speed Channel)						
Input logic high level	V_{IH}	VCC=3.3~5.5V	1.6			V
		VCC=1.5~3.3V	1.4			V
Input logic low level	V_{IL}	VCC=3.3~5.5V			0.6	V
		VCC=1.5~3.3V			0.4	V
Supply quiescent current	I_{CC}	I_A=0, V_{SEL} =0 or V_{SEL} =VCC			2.0	uA
Increase in I_{CC} per input	I_{CCT}	I_A=0, VCC=4.5V V_{SEL}>1.8 or V_{SEL}<0.5			2.0	uA
Off state leakage from A1 to B01 (or B11)	I_A	V_A = 5.5V , $V_{B01(or\ B11)}$ = 0V			±2.0	uA
Off state leakage from A2 to B02 (or B12)	I_A	V_A = 5.5V , $V_{B02(or\ B12)}$ = 0V			±2.0	uA
On-Resistance	R_{ON1}	V_A=0 ~ 0.5V, I_A=30mA		3.0	3.5	Ω
	R_{ON2}	V_A=0.5 ~ 2.0V, I_A=30mA		3.6	3.9	Ω
	R_{ON3}	V_A=2.0 ~ 4.0V, I_A=30mA		2.5	3.5	Ω
	R_{ON4}	V_A=4.0 ~ 5.5V, I_A=30mA		1.5	1.8	Ω
On-Resistance Flatness	R_{FLAT1}	V_A=0 ~ 0.5V, I_A=30mA		0.7		Ω
	R_{FLAT2}	V_A=0.5 ~ 2.0V, I_A=30mA		0.5		Ω
	R_{FLAT3}	V_A=2.0 ~ 4.0V, I_A=30mA		1.6		Ω
	R_{FLAT4}	V_A=4.0 ~ 5.5V, I_A=30mA		0.3		Ω
On-Resistance Matching Between Channels	Δ R_{ON}	V_A=0~5.5V, I_A=30mA		0.1	0.2	Ω
AC CHARACTERISTICS (Normal Speed Channel)						
Turn-On Time	T_{ON}	V_A=1.5V, C_L=35pF, RL=50Ω		200		nS
Turn-Off Time	T_{OFF}	V_A=1.5V, C_L=35pF, R_L=50Ω		200		nS
Break-Before-Make time	T_{BBM}	V_A=1.5V, C_L=35pF, R_L=50Ω		500		nS
-3dB Bandwidth	BW	R_L=50Ω, C_L=0pF		700		MHZ
Off isolation	OIRR	F=1KHz, R_L=50Ω		-81		dB
		F=10KHz, R_L=50Ω		-80		dB
Crosstalk	Xtalk	F=1KHz, R_L=50Ω		-83		dB
		F=10KHz, R_L=50Ω		-82		dB
Total Harmonic Distortion	THD	F=20Hz to 20KHz V_A=600mVp-p @R_L=32Ω,		-80		dB
CAPACITANCE (Normal Speed Channel)						
Off capacitance	C_{OFF}	F=100KHz, VCC=3.3		5		pF
On capacitance	C_{ON}	F=100KHz, VCC=3.3		7		pF

Notes:

(1) Flatness is defined as the difference between maximum and minimum value of ON-resistance at the specified analog signal voltage points.

(2) R_{ON} matching between channels is calculated by subtracting the channel with the lowest max Ron value from the channel with the highest max Ron value.

(3) Crosstalk is inversely proportional to source impedance

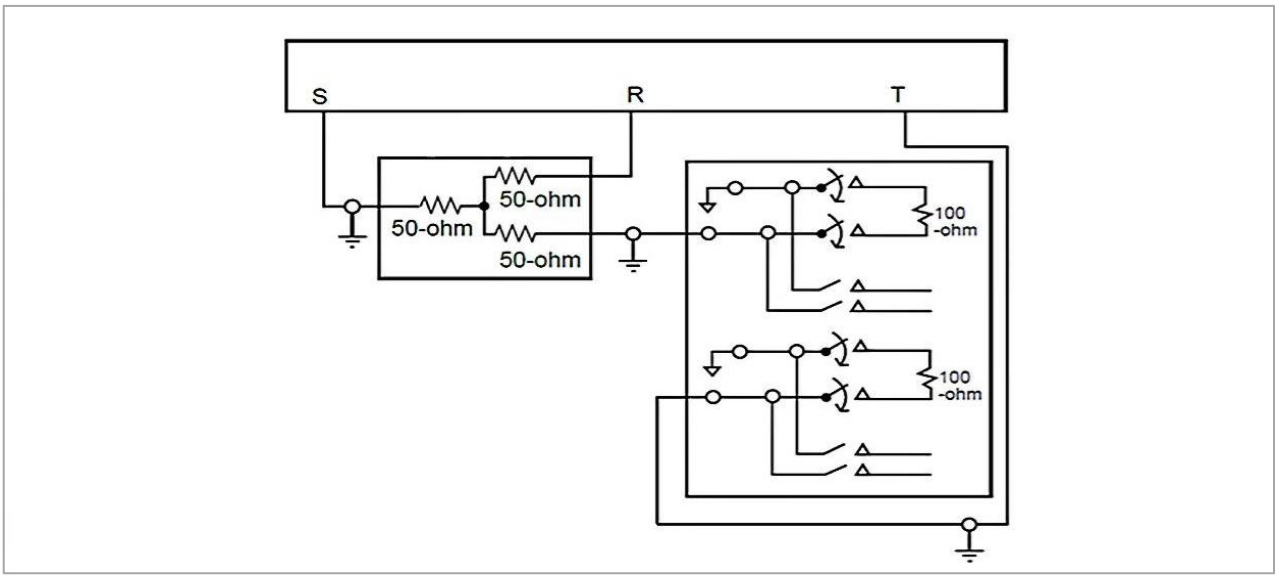


Fig.1 Crosstalk Setup

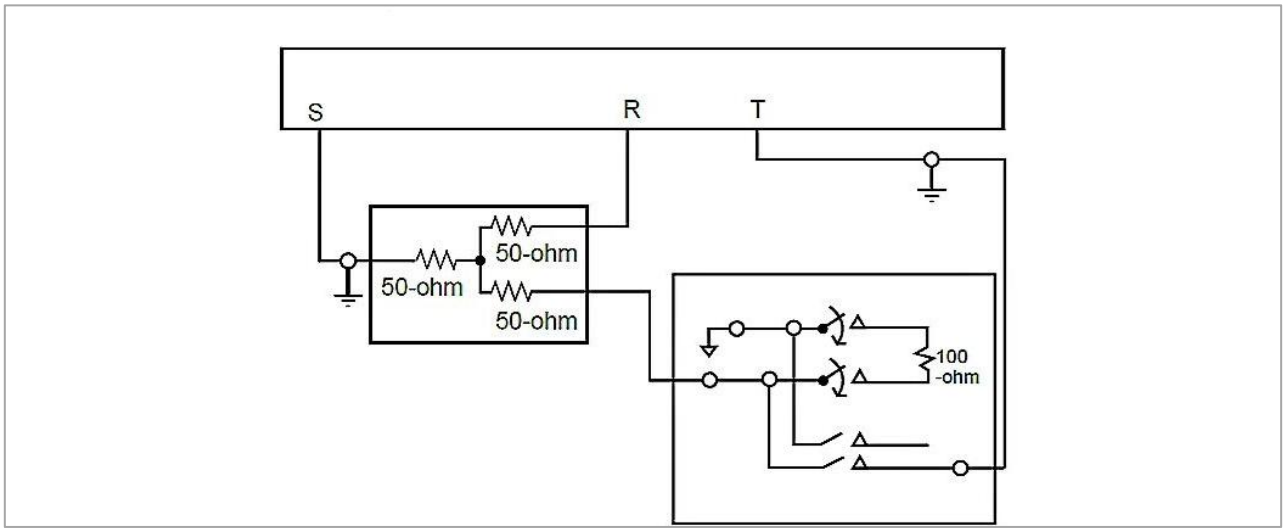
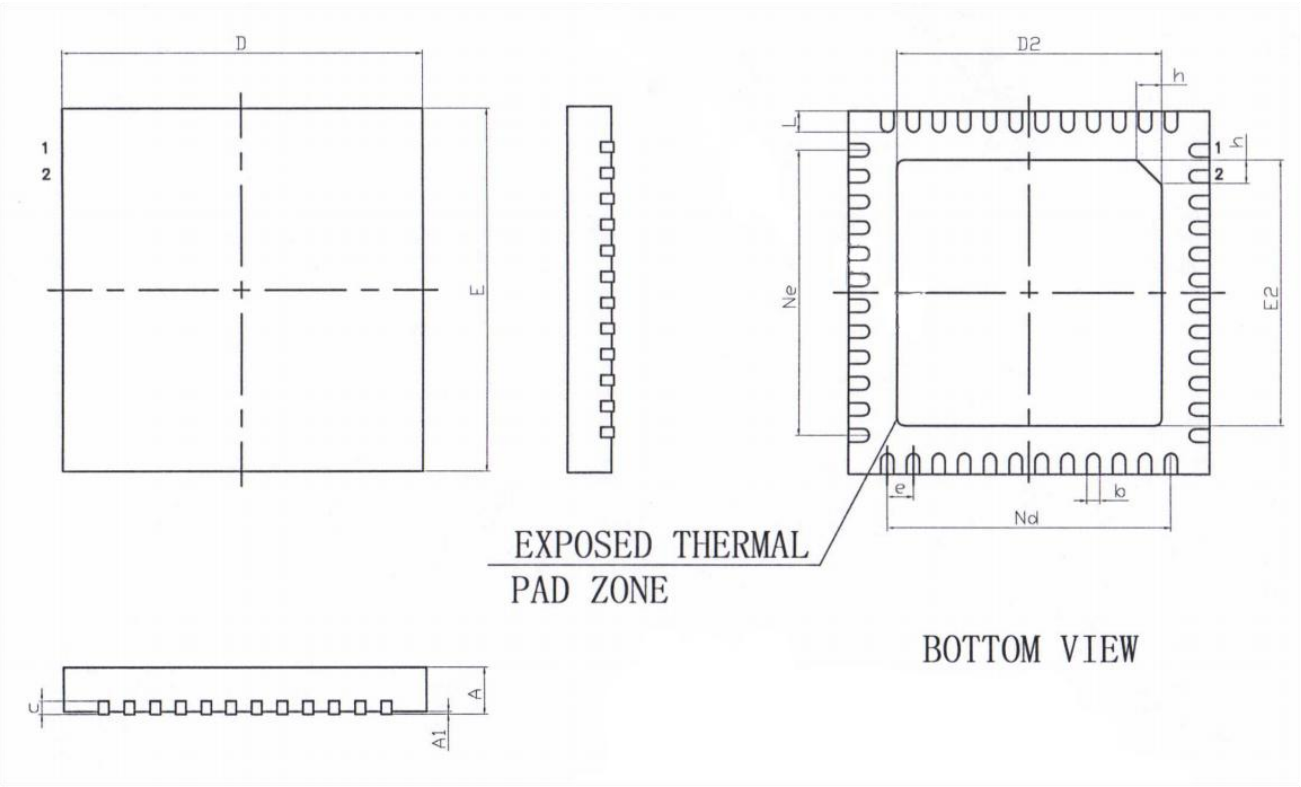


Fig.2 OFF-isolation

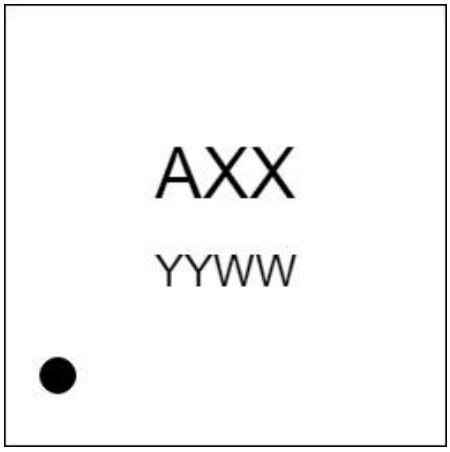
Package Outline Dimensions(All dimensions in mm.)

(1) Package Type: QFN6x6-48L



SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	0.70	0.75	0.80	
A1	—	0.02	0.05	
b	0.15	0.20	0.25	1
c	0.18	0.20	0.23	
D	5.90	6.00	6.10	
D2	4.10	4.20	4.30	2
e	0.40BSC			
Ne	4.40BSC			
Nd	4.40BSC			
E	5.90	6.00	6.10	
E2	4.10	4.20	4.30	2
L	0.35	0.40	0.45	
h	0.30	0.35	0.40	
L/F载体尺寸 (MIL)	177*177			

(2) Top Marking Information



YY: Year (23=2023,24=2024…)

WW: Weekly (01-53)

AXX: Imternal ID Code

Version Modification Record

Version Number	Revision	Date
first edition		/
V1.0	1. Update the Pin Configuration on page 2&3 2. Update the test condition and “On-Resistance for TX/RX” of “Electrical Characteristics” on page 6	2024/07/18
V2.0	1.Update the “Pin Configuration” on page 2	2024/08/14
V3.0	1.Update the “Order information”on page 2	2024/08/22